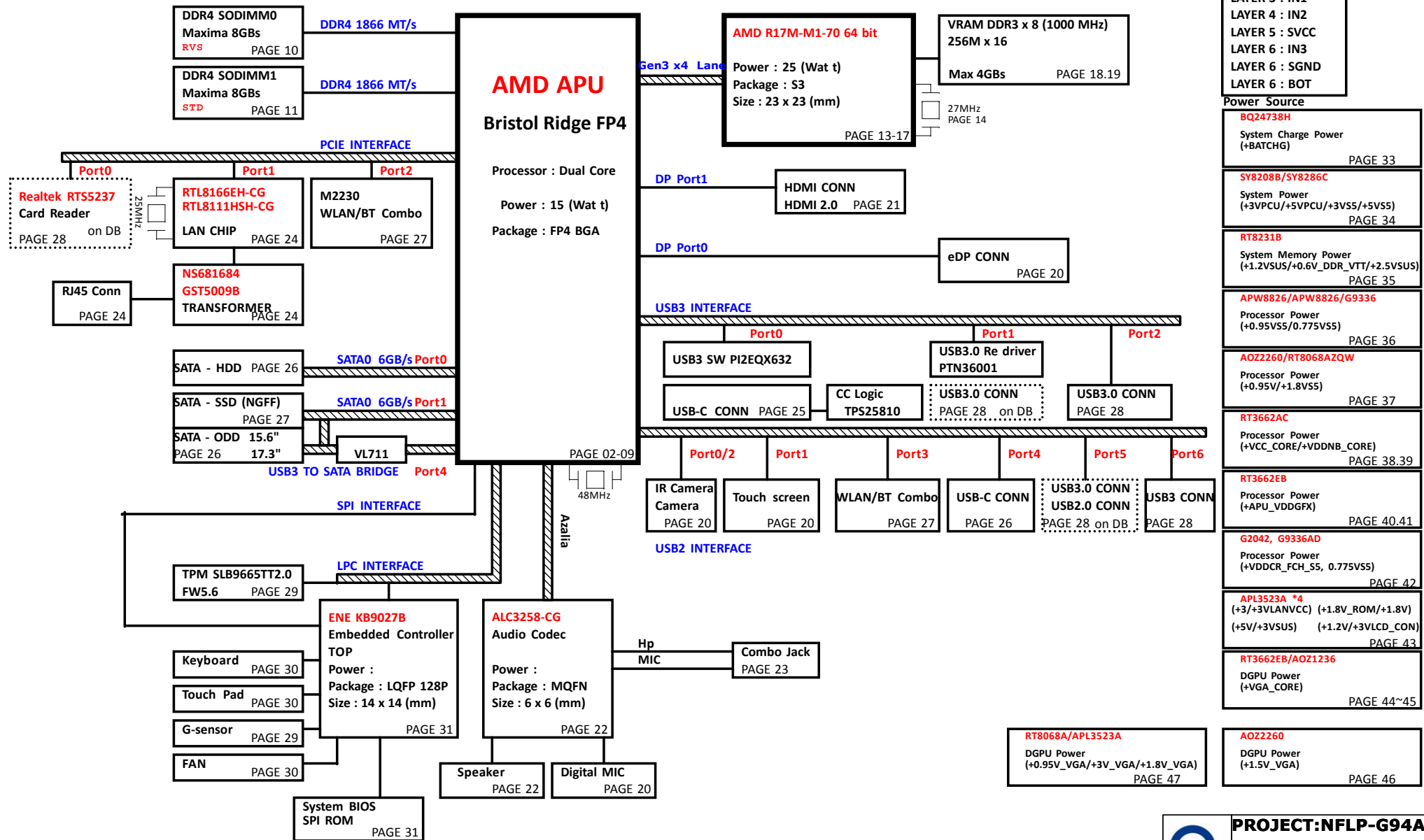
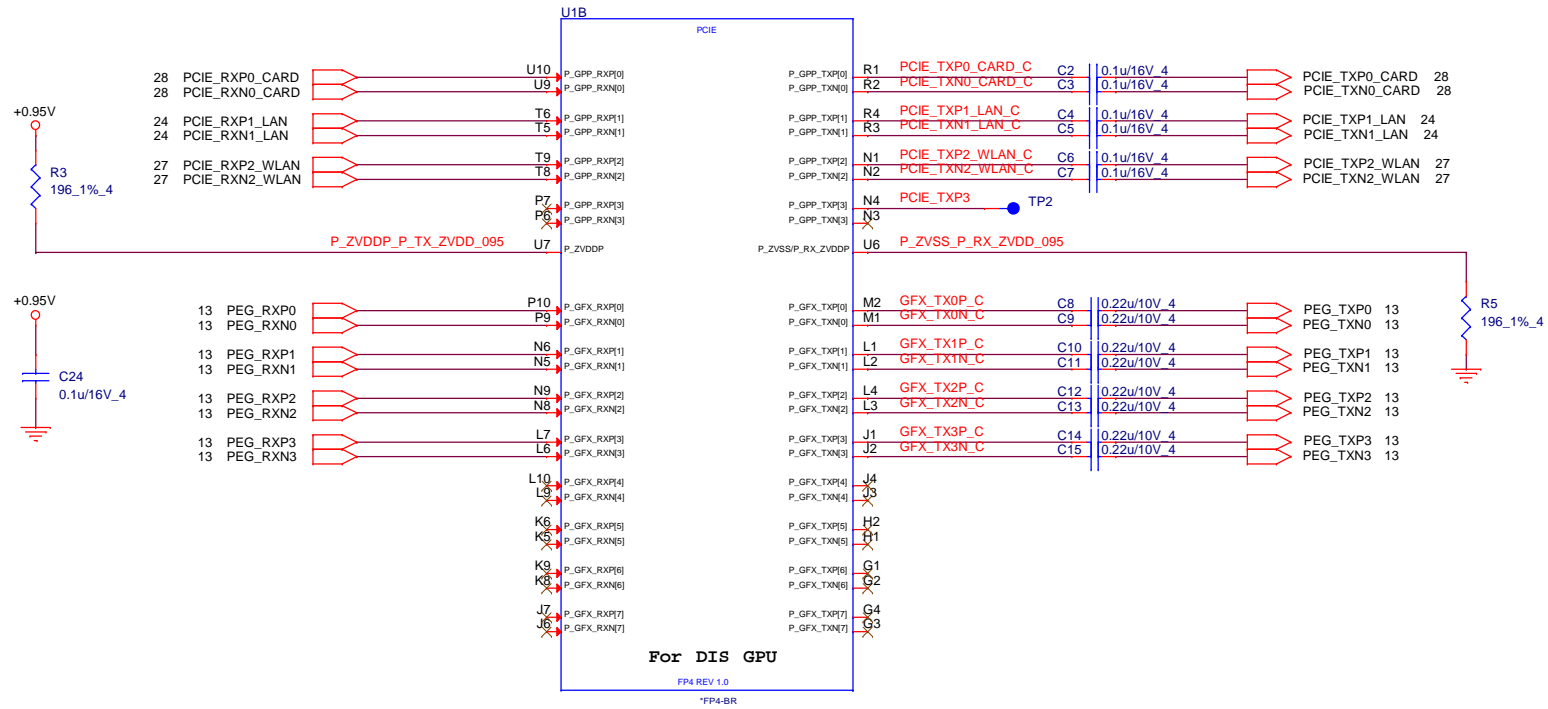


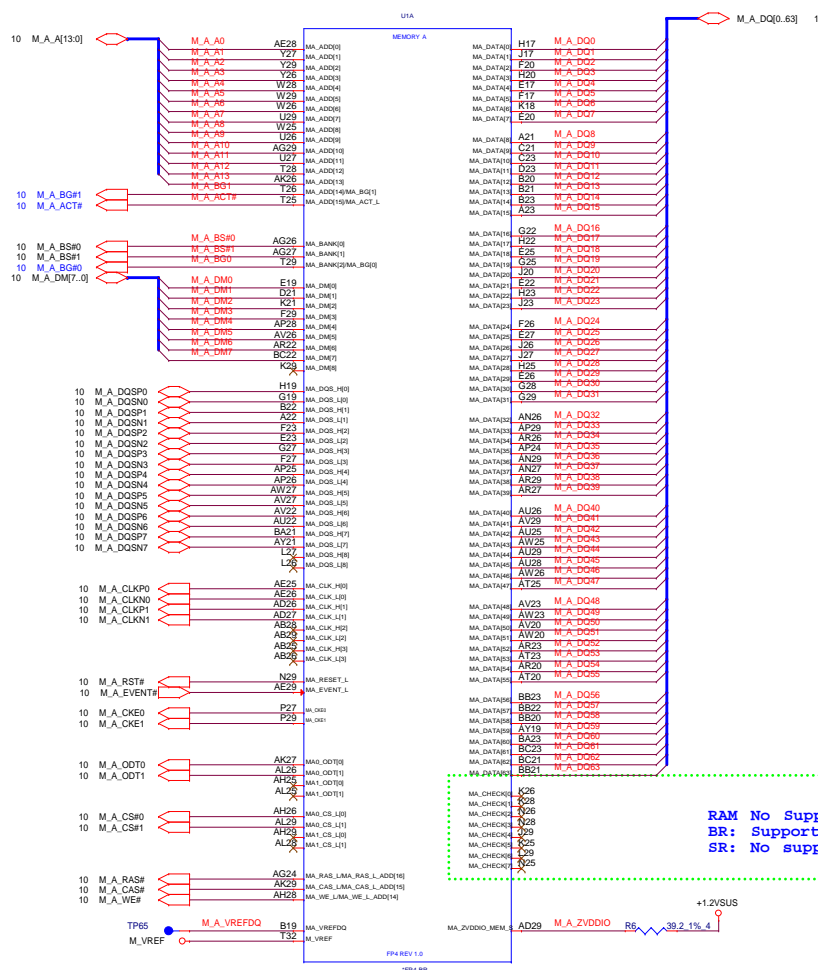
G94A 15.6"/17.3" 2SPD System Block Diagram-AMD Bristol FP4 01



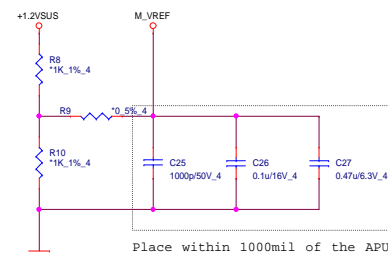


PROJECT:NFLP-G94A			
Quanta Computer Inc.			
Size	Document Number		Rev
	BR & SR 1/7(PCIE)		1A
Date: Monday, January 16, 2017		Sheet 2 of 48	

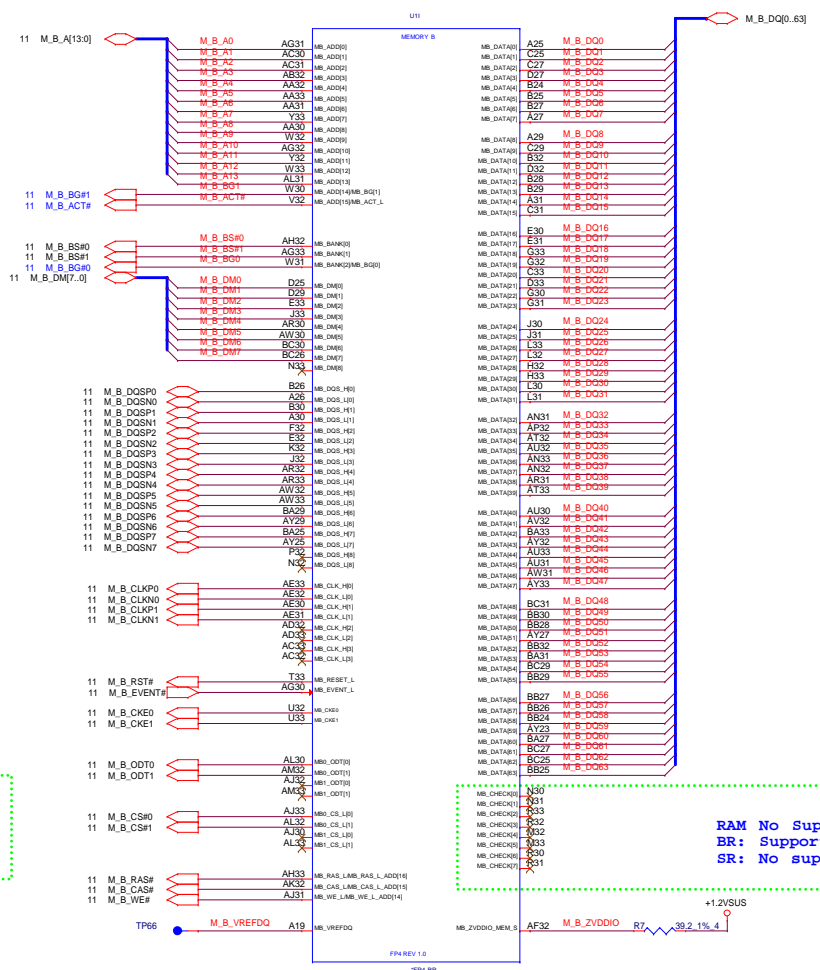
SB only channel B



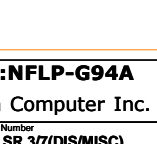
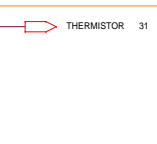
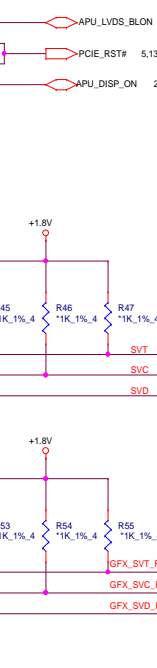
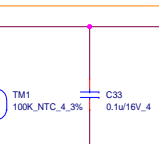
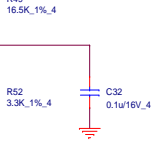
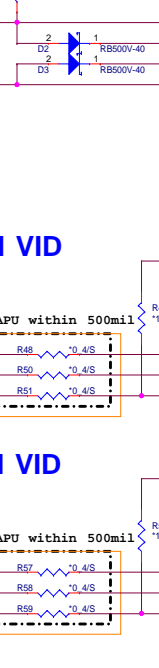
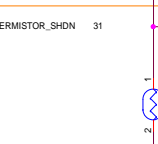
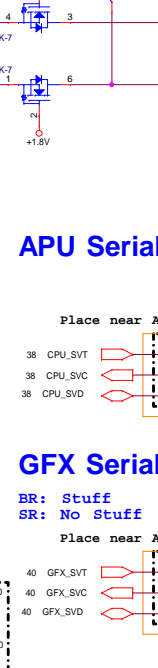
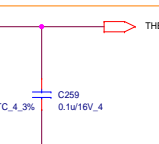
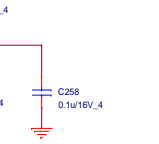
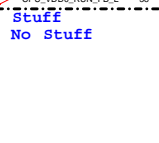
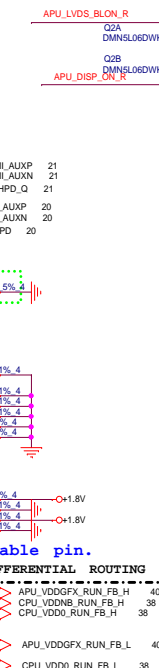
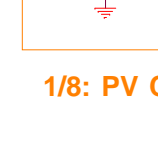
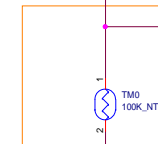
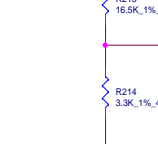
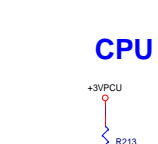
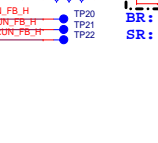
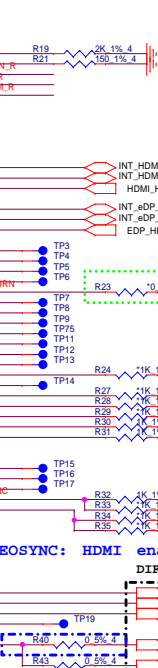
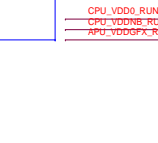
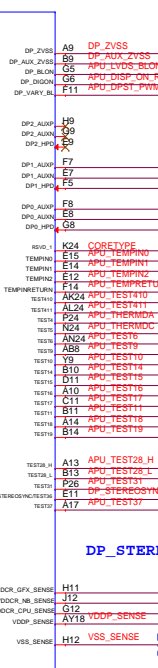
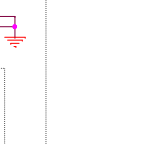
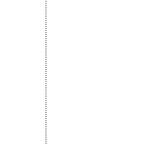
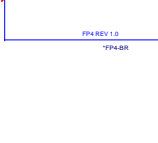
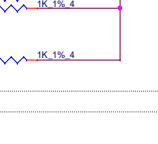
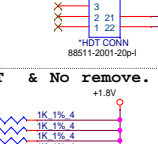
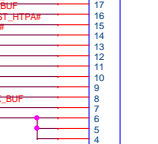
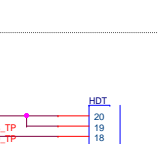
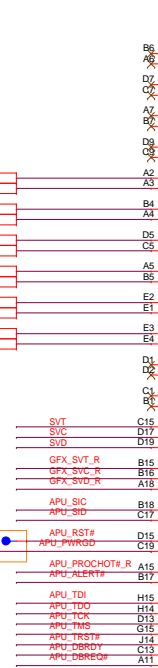
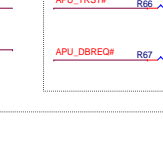
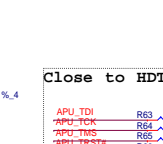
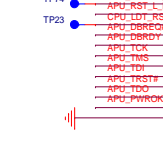
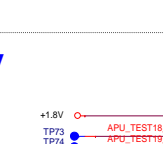
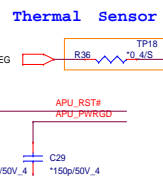
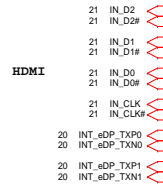
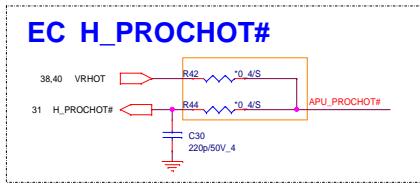
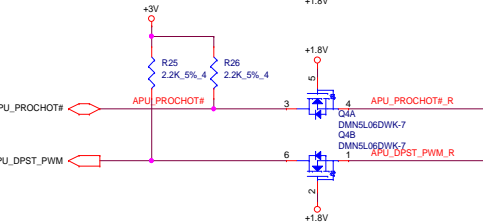
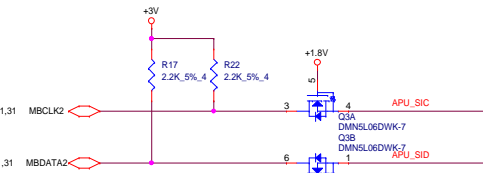
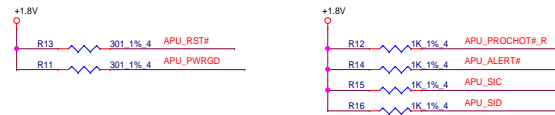
```
RAM No Support
BR: Support ECC
SR: No support ECC
```



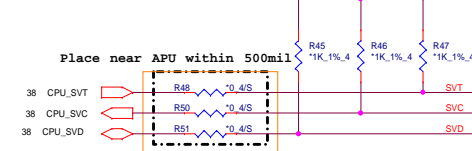
Place within 1000mil of the APU



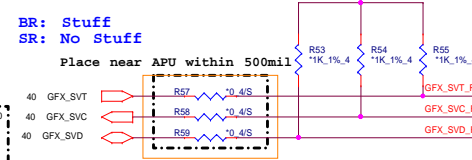
```
RAM No Support
BR: Support ECC
SR: No support ECC
```



APU Serial VID

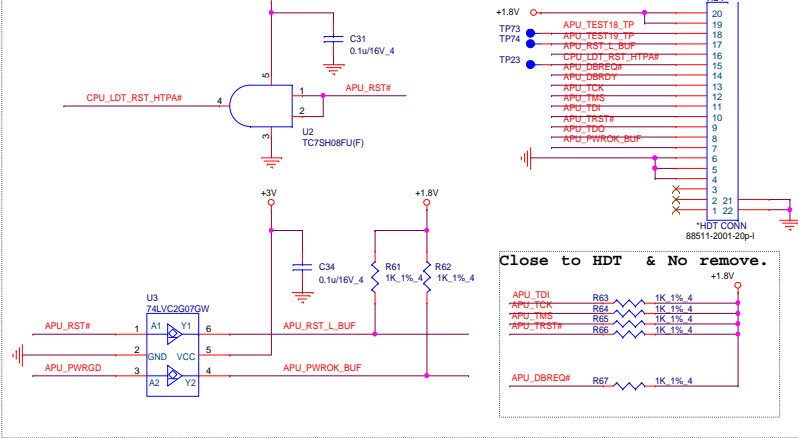


GFX Serial VID

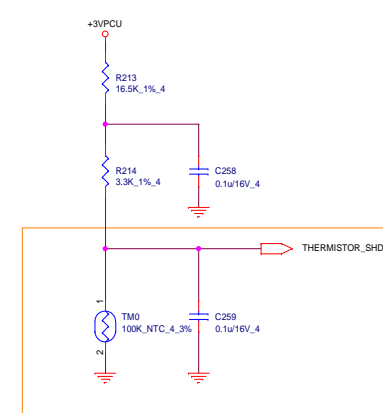


HDT+ Connector for Debug only

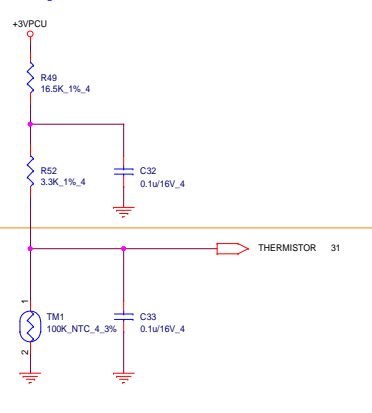
Can remove on MP



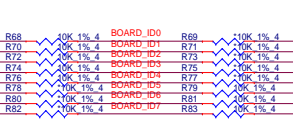
CPU Thermal Protect



Pipe Thermal Protect



1/8: PV Change net name



Board ID 0	Definition
0	UMA
1	DIS

Board ID [2:1]	Definition
00	14"
01	15.6" 1SPD
10	17"
11	15.6" 2SPD

Board ID [4:3]	Definition
00	PORT0 SATA only
01	PORT0 SATA PORT1 SSD
10	PORT0 SATA PORT1 ODD
11	PORT0 SATA PORT1 SSD USB3.0 to ODD
Board ID [5]	Definition
0/1	BR/SR

Board ID [6]	Definition
0/1	VRAM Size X8/ X4

Board ID [7]	GPU
0/1	M1-70/ M1-30

Board ID [9:8]	Definition
00	NFL-P
01	NFL-C
10	VINE-DF
11	Reserve
Board ID [10]	Definition
0/1	Reserve

22 ACZ_SDOUT_AUDIO \leftarrow R119 33 5% \rightarrow ACZ_SDOUT_R

22 ACZ_SYNC_AUDIO \leftarrow R120 33 5% \rightarrow ACZ_SYNC_R

22 BIT_CLK_AUDIO \leftarrow R121 33 5% \rightarrow ACZ_BCLK_R

22 ACZ_RST#_AUDIO \leftarrow EC1 50pF 150V50V \rightarrow ACZ_RST#_R

22 ACZ_SDI#0 \leftarrow R122 33 5% \rightarrow ACZ_SDI#0

31,44,7 DGPU_PR_EN

R176 1k

2

C43 0.47uF 6.3V_4

Q5 MTRX213-G

3

CLKREQ#

DIS: Stuff
UMA: No Stuff

38 CPU_VRM8380_PG

31 ECPWR0K

D1

1

2

3

BAT54AW-L

10K,1%,4

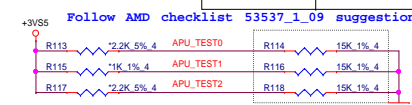
R124

4S

C42

*2.2u/10V_4

SYS_PWRGD



TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted. FCH JTAP pins are overloaded for multiple functions, in this configuration the FCH JTAP are used as non-JTAP pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAP multi-function pins are configured as JTAP pins, in this configuration the FCH TAP can be accessed from FCH JTAP pins
1	TMS	1	Use on ATE only Yuba JTAP enabled

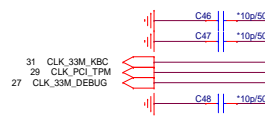
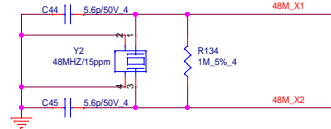
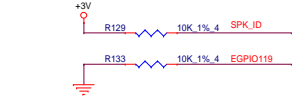
5,7,25,27,30,31,34,35,37,42,43,44,47
7,36,42
4,5,7,10,11,20,21,22,24,26,27,28,29,30,31,38,40,43
7,31,43

+3VS5
+0.95VS5
+3V
+1.8V_ROM



Follow Checklist

OPTION: ODD or SSD(M.2)

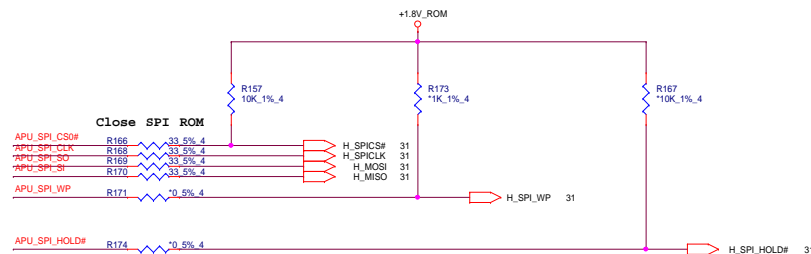


For EMI



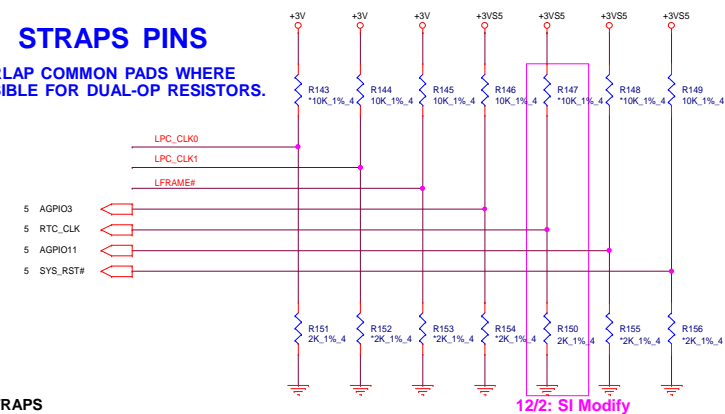
APU SPI ROM

Vender	Size	P/N (1.8V)
WND	8M	AKE5E2N0N00
EON	8M	AKE5EFN0Q00
	8M	
Socket	DFHS08FS023	



STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

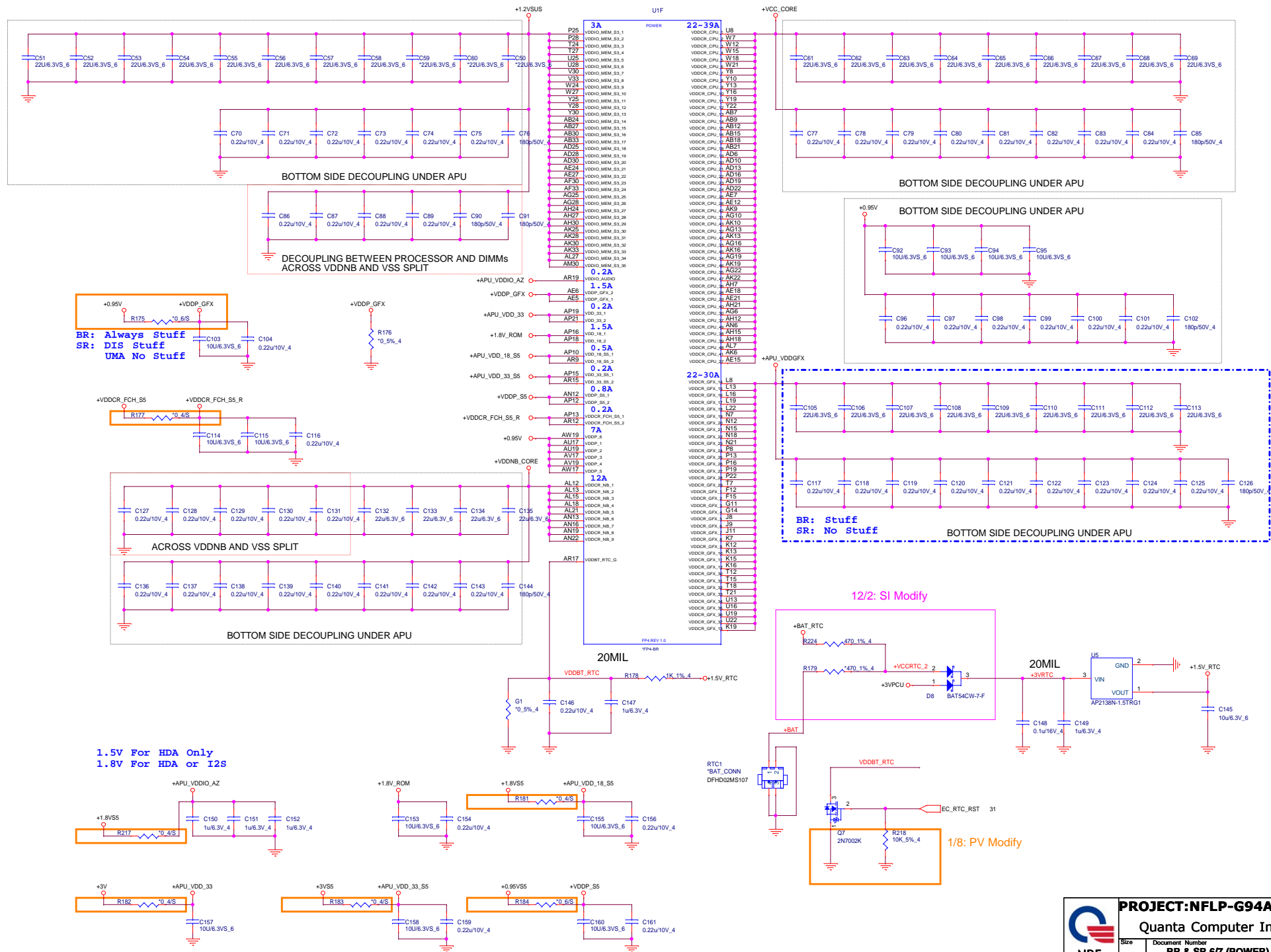
	LPC_CLK0	LPC_CLK1	LFRAME#	AGPIO3 Int Pull-Up	RTC_CLK Int Pull-Up	AGPIO11=BLINK Int Pull-Up	SYS_RST# Int Pull-Up
PULL HIGH	BOOT FAIL TIMER ENABLED	Use 48Mhz crystal clock and generate both internal and external clocks DEFAULT	SPI ROM DEFAULT	1.8V SPI ROM Enhanced reset logic (for quicker S5 resume) DEFAULT	Coin battery is on board. DEFAULT	LDT_RST#/LDT_PWRGD output to APU DEFAULT	normal reset mode DEFAULT
PULL LOW	BOOT FAIL TIMER DISABLED DEFAULT	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	LPC ROM	3.3V SPI ROM Default to traditional reset logic DEFAULT	Coin battery is not on board.	LDT_RST#/LDT_PWRGD output to Pads	short reset mode

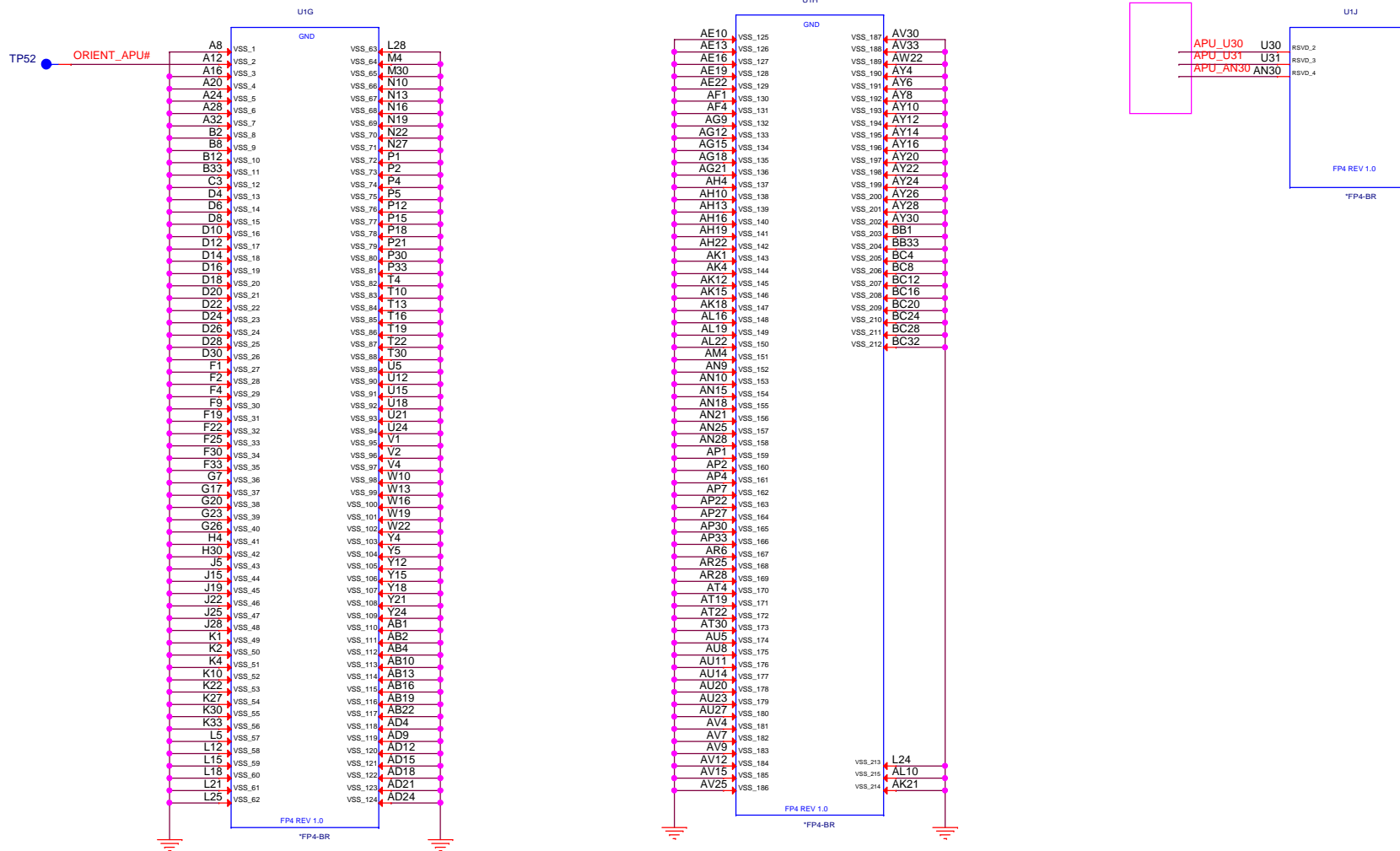


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Quanta Computer Inc.

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	BR & SR 5/7(SATA/USB/SPI)	1A
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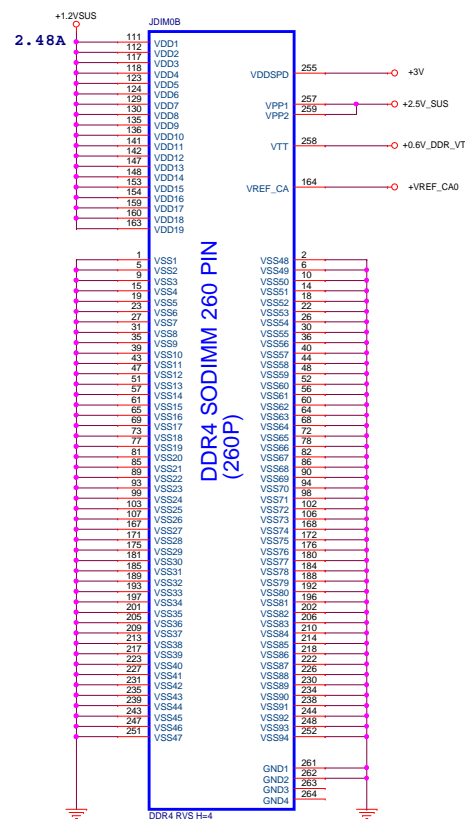
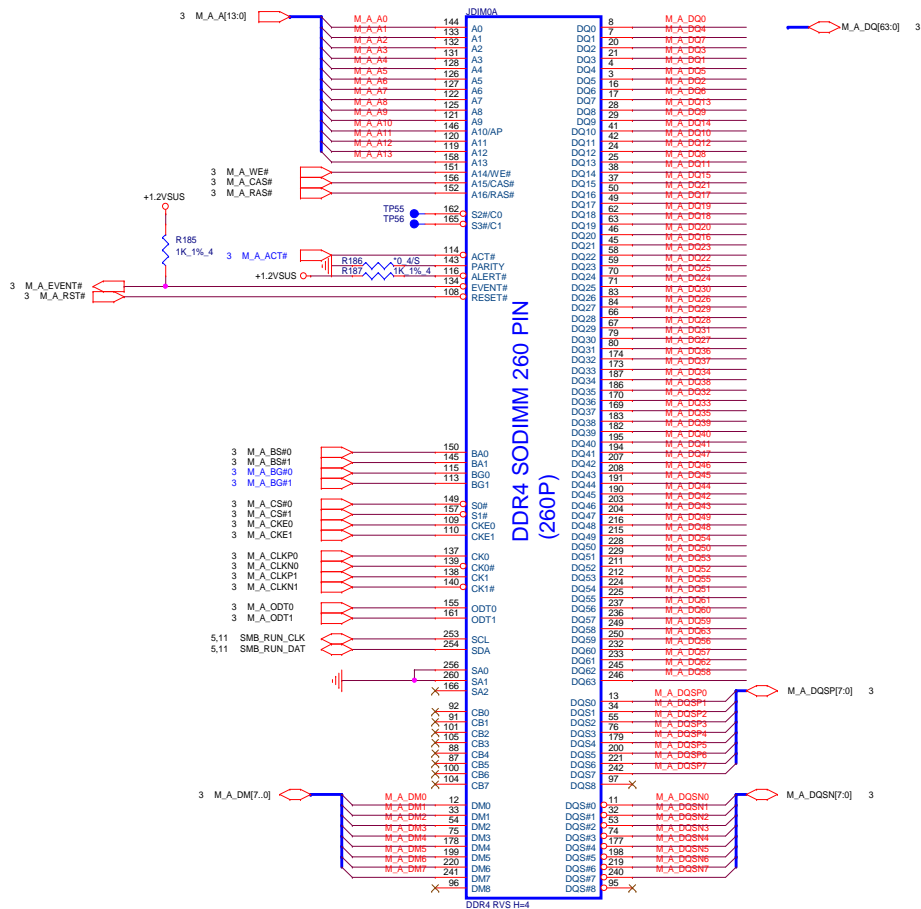


**PROJECT:NFLP-G94A**

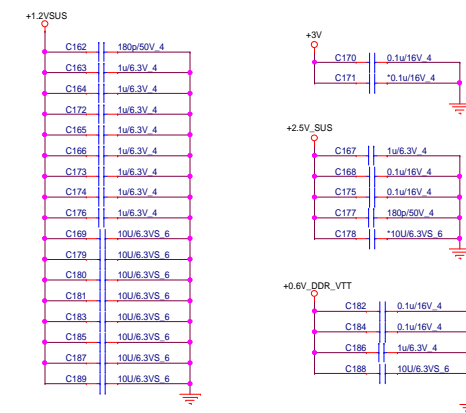
Quanta Computer Inc.

Size	Document Number	Rev
	BR & SR 7/7 (GND)	1A
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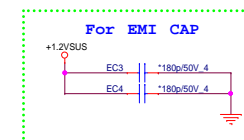
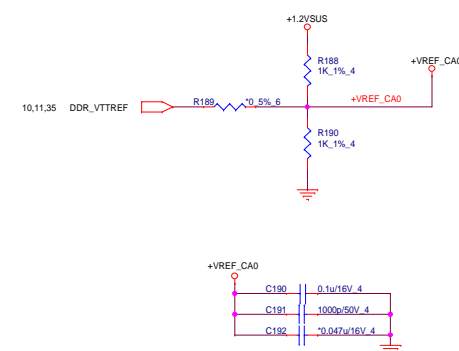
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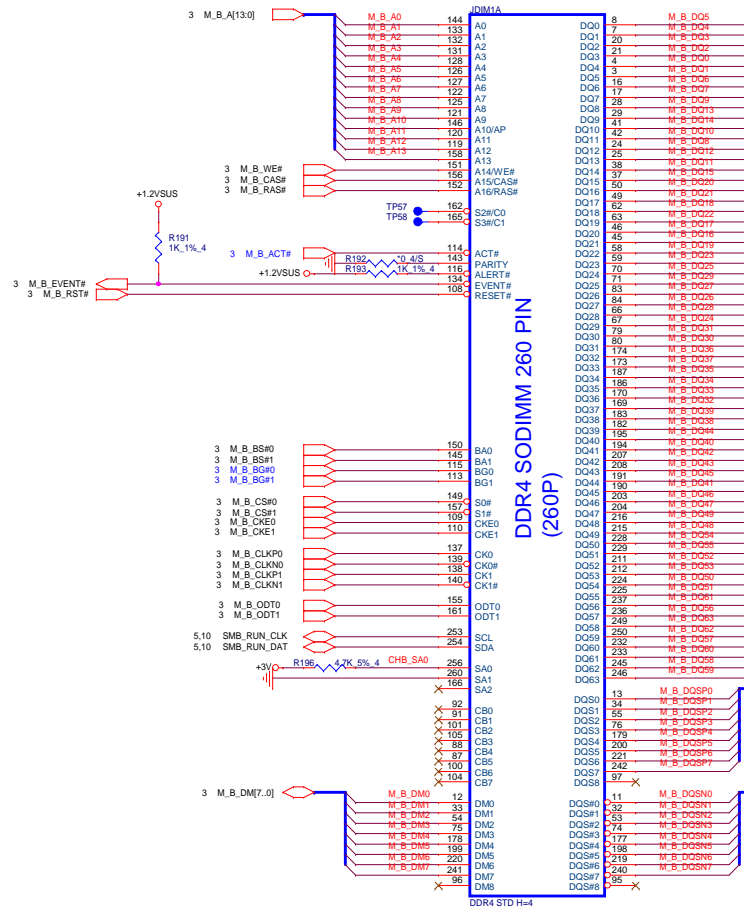


Place these Caps near SODIMM



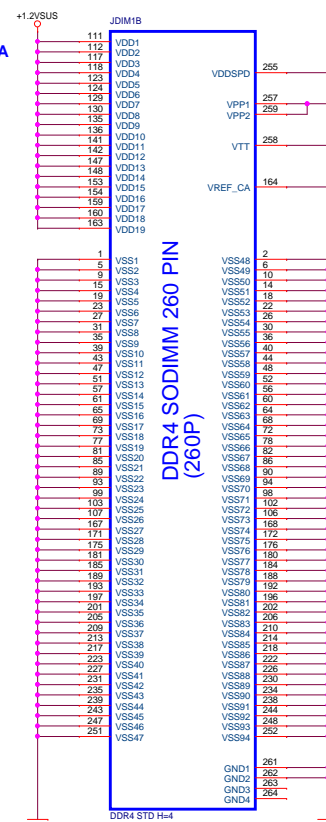
1uF/10uF 4pcs on each side of SODIMM





M.B. DQ[63:0]

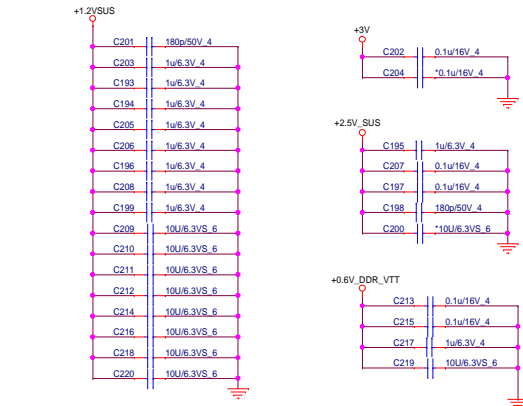
2.48A



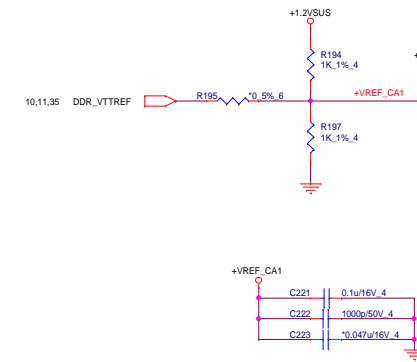
DDR4 SODIMM 260 PIN (260P)

DDR4 STD H=4

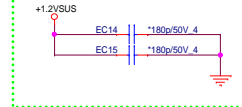
Place these Caps near SODIMM



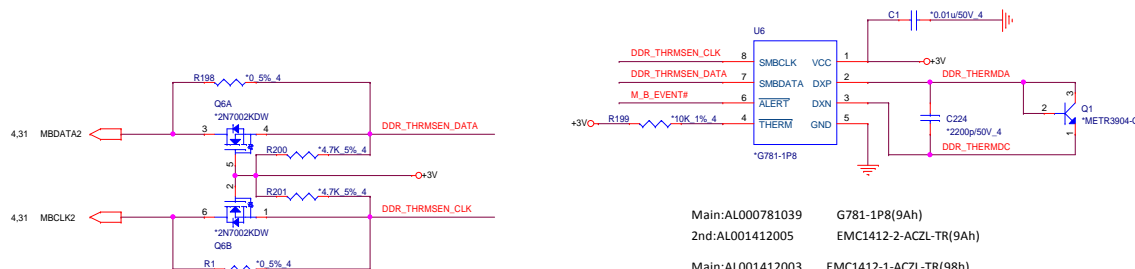
1uF/10uF 4pcs on each side of SODIMM



For EMI CAP

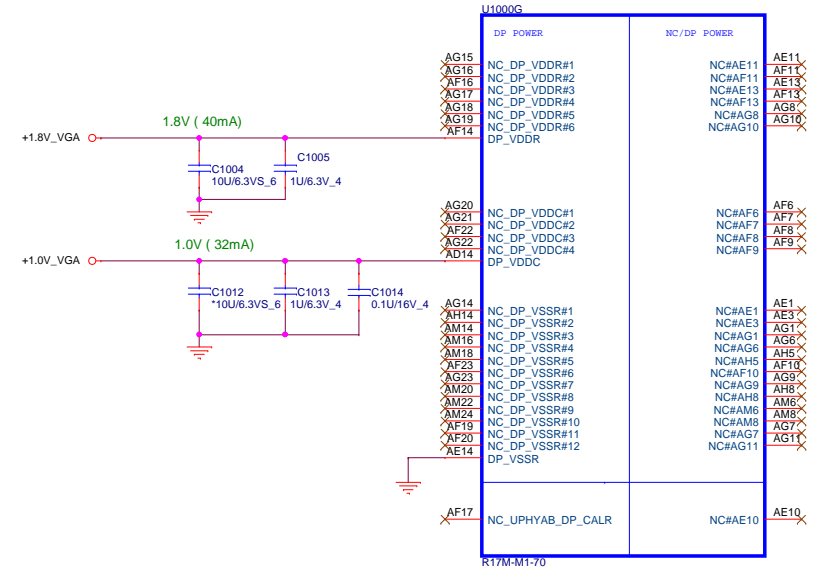
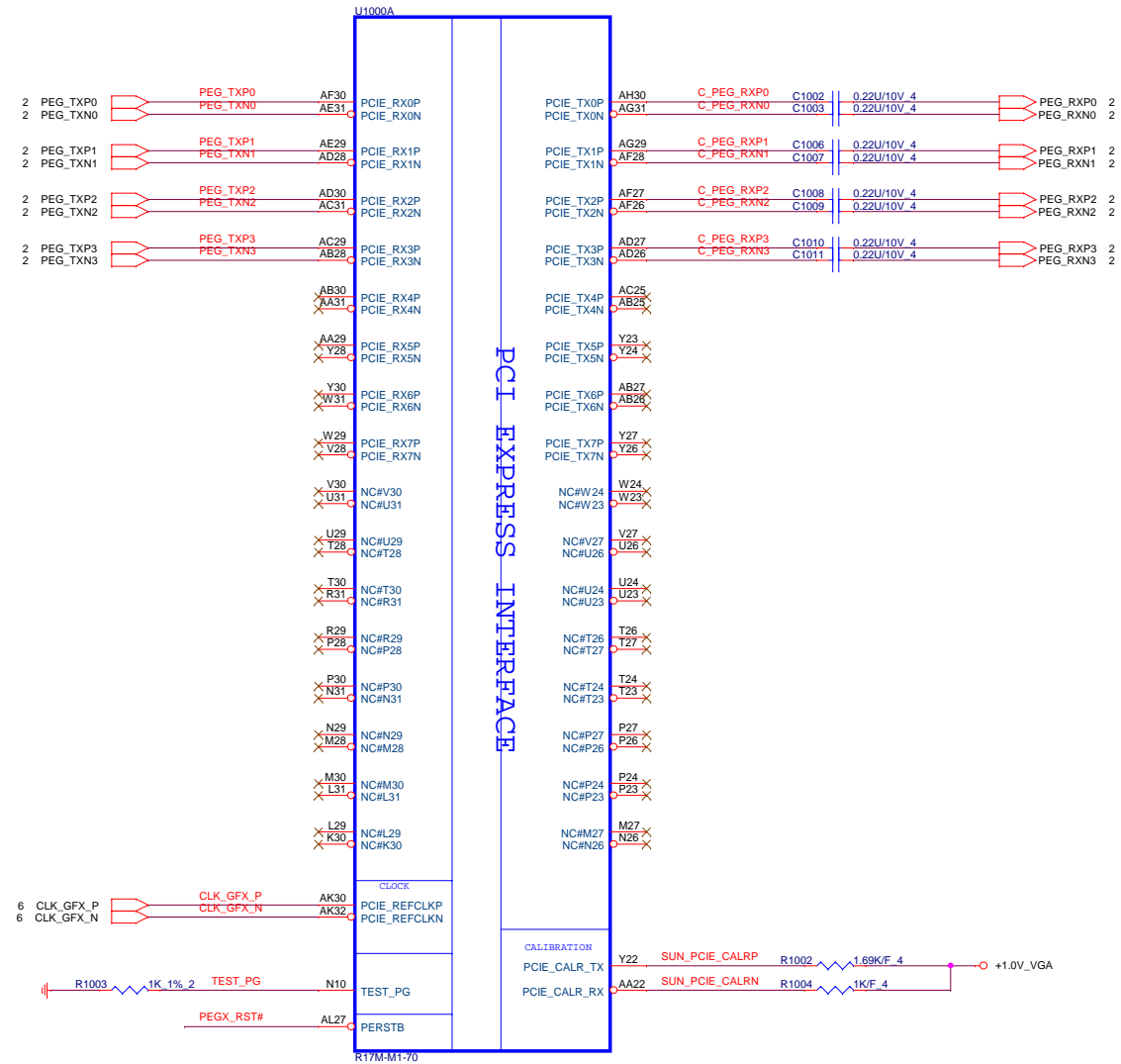


Local Thermal Sensor

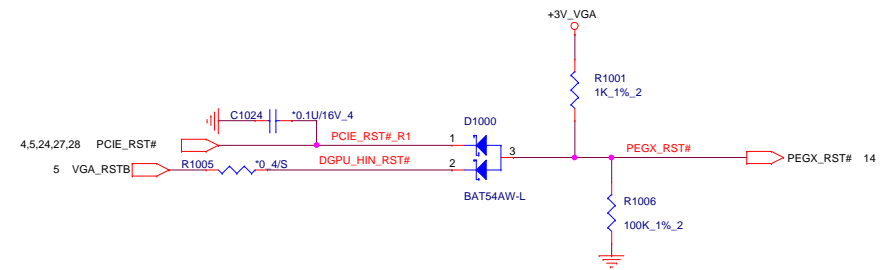


Main:AL000781039 G781-1P8(9Ah)
 2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)
 Main:AL001412003 EMC1412-1-ACZL-TR(98h)
 2nd:AL000431014 TMP431ADGKR(98h)

14,16,43,44,47 +3V_VGA
14,16,43,44,47 +1.8V_VGA
16,43,47 +1.0V_VGA



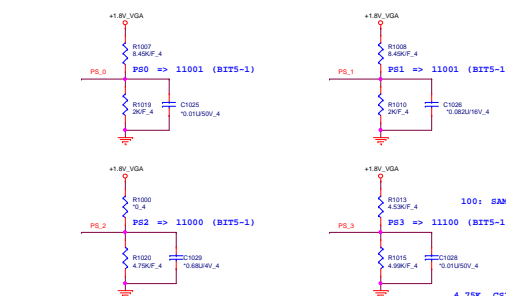
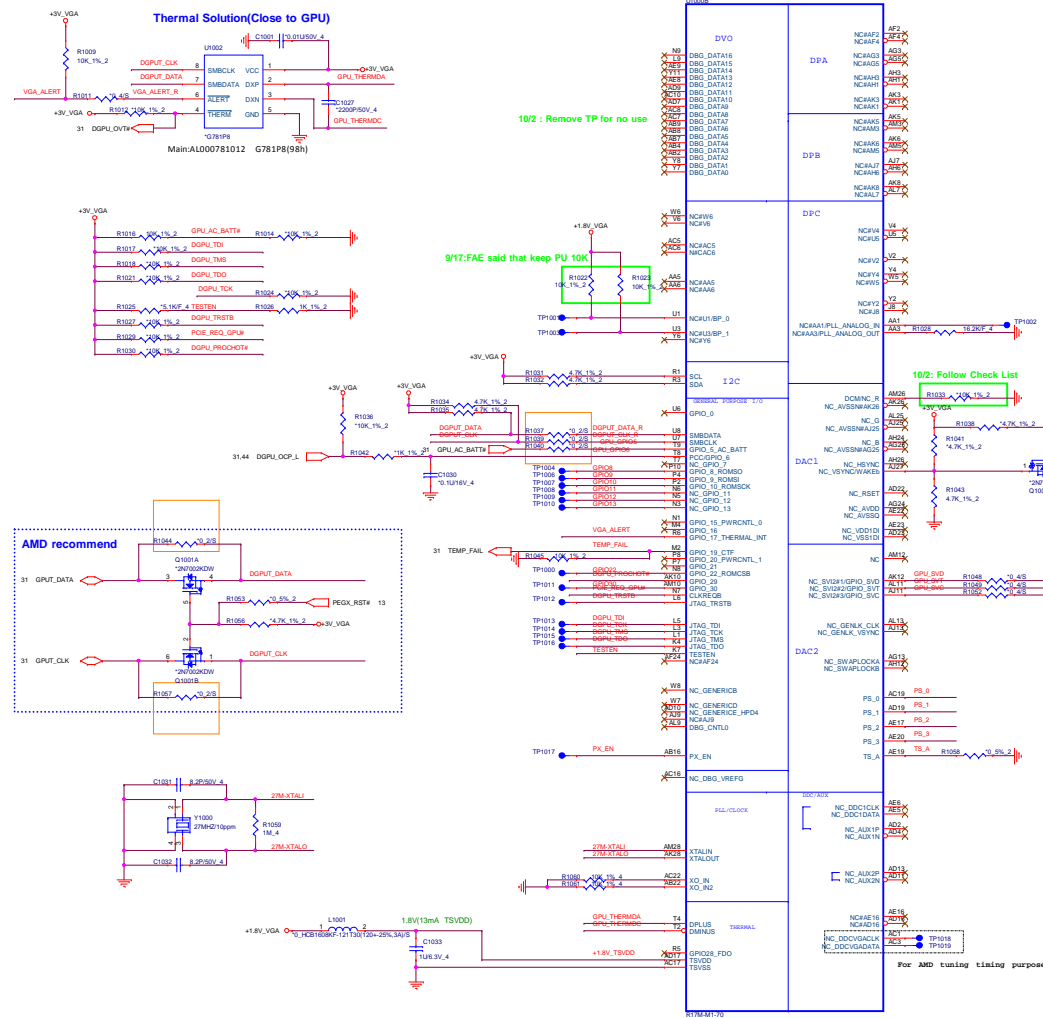
GPU Reset Signal



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PS_3[3:1]	Vendor	Type	Vendor P/N	PU	PD
000	Micron	256Mx16 *4, 1000mV	H74J256N16LY-091G1N	NC	4.75K
001	Samsung	256Mx16 *4, 1000mV	K4W401646E-BC1A	8.45K	2.00K
010	Hynix	256Mx16 *4, 1000mV	H57C4G63BFR-N0C	4.53K	2.00K
011	Micron	256Mx16 *8, 1000mV	H74J256N16LY-091G1N	6.98K	4.99K
100	Samsung	256Mx16 *8, 1000mV	K4W401646E-BC1A	4.53K	4.99K
101	Hynix	256Mx16 *8, 1000mV	H57C4G63BFR-N0C	3.24K	5.62K

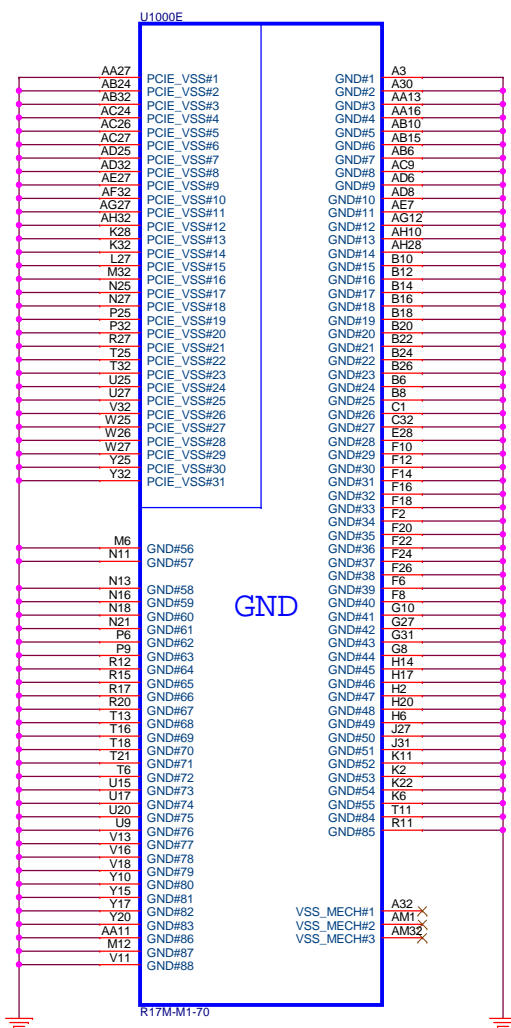
- PS PS Implementation**
- Connect GPD_2B to 10K pull-down to enable HUPS.
 - Pin of PS_0, PS_1, PS_2 is not used, leave "No connect".
 - R, pu, R, pd and C must be properly populated per tables below.
 - Place HUPS circuit component as close to the PS pin as possible.
 - Total DC resistance of trace between PS pin and C should be less than 2 ohms.
 - Total DC resistance of trace between C and ground should be less than 2 ohms.
 - Trace capacitance should be less than 100pF. Resistor should be of +/-1% tolerance.

Capacitor Loading Table		Resistor Divider Loading	
C (pF)	SW(C,A)	R _{pu} (Ohm)	R _{pd}
000	00	NC	47
01	01	8450	20
10	10	4530	20
NC	11	6980	40
		4530	49
		3240	56
		3400	100

Table 3-24 Primary Memory Aperture Sizes Requested at PCI Configuration

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011
512 MB	Not Supported
1 GB	Not Supported
2 GB	Not Supported
4 GB	Not Supported

NLPS pin	Strap Name	Description	Recommended Settings
PS_H01	ROM_CONFIG[0]	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[0] follows the ROM type.	Design dependent, use the description.
PS_H02	ROM_CONFIG[1]	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[1] follows the primary memory aperture size. See Table 3-24 Primary Memory Aperture Sizes.	Design dependent, use the description.
PS_H03	ROM_CONFIG[2]	Reserved for internal use only. Must be 1 at reset.	1
PS_H04	N/A	Reserved.	1
PS_H101	STRAP_BIF_GEN0_EN_A	1 = PCIe GEN3 capabilities. 0 = PCIe GEN3 is not supported.	Design dependent, use the description.
PS_H102	STRAP_BIF_CLK_PN_EN	1 = The CLKREQ# power management capability is disabled. 0 = The CLKREQ# power management capability is enabled.	0
PS_H103	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_H104	STRAP_TX_CFG_DRV_FULL_SWING	1 = The transmitter full-swing is enabled. 0 = The transmitter full-swing is disabled.	1
PS_H105	STRAP_TX_DEEMPH_EN	1 = Tx deemphasis enabled. 0 = Tx deemphasis disabled.	Design dependent, use the description.
PS_H106	N/A	Reserved.	0
PS_H107	N/A	Reserved.	0
PS_H201	STRAP_BIOS_ROM_EN	1 = Enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device.	Design dependent, use the description.
PS_H202	N/A	Reserved.	0
PS_H203	N/A	Reserved.	0
PS_H204	N/A	Reserved.	0
PS_H205	N/A	Reserved.	0
PS_H301	BOARD_CONFIG[0]	Board configuration related information, such as memory ID.	Design dependent, use the description.
PS_H302	BOARD_CONFIG[1]	Board configuration related information, such as memory ID.	Design dependent, use the description.
PS_H303	N/A	Reserved.	0
PS_H304	N/A	Reserved.	0



CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

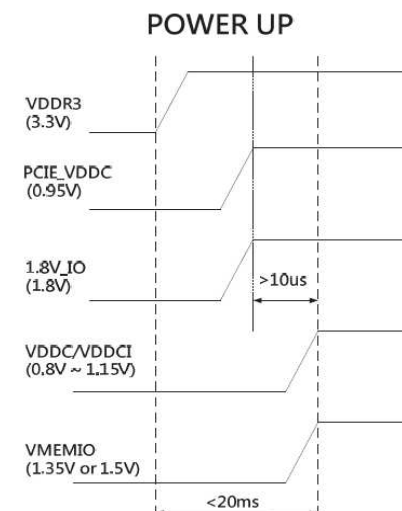
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSXNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

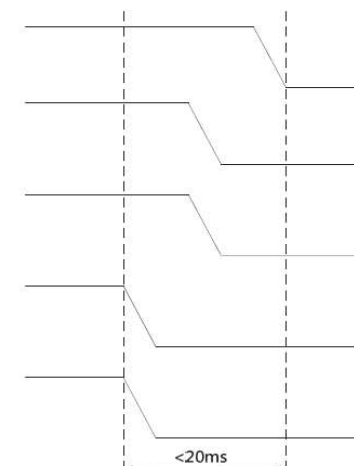
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

POWER UP / POWER DOWN SEQUENCE



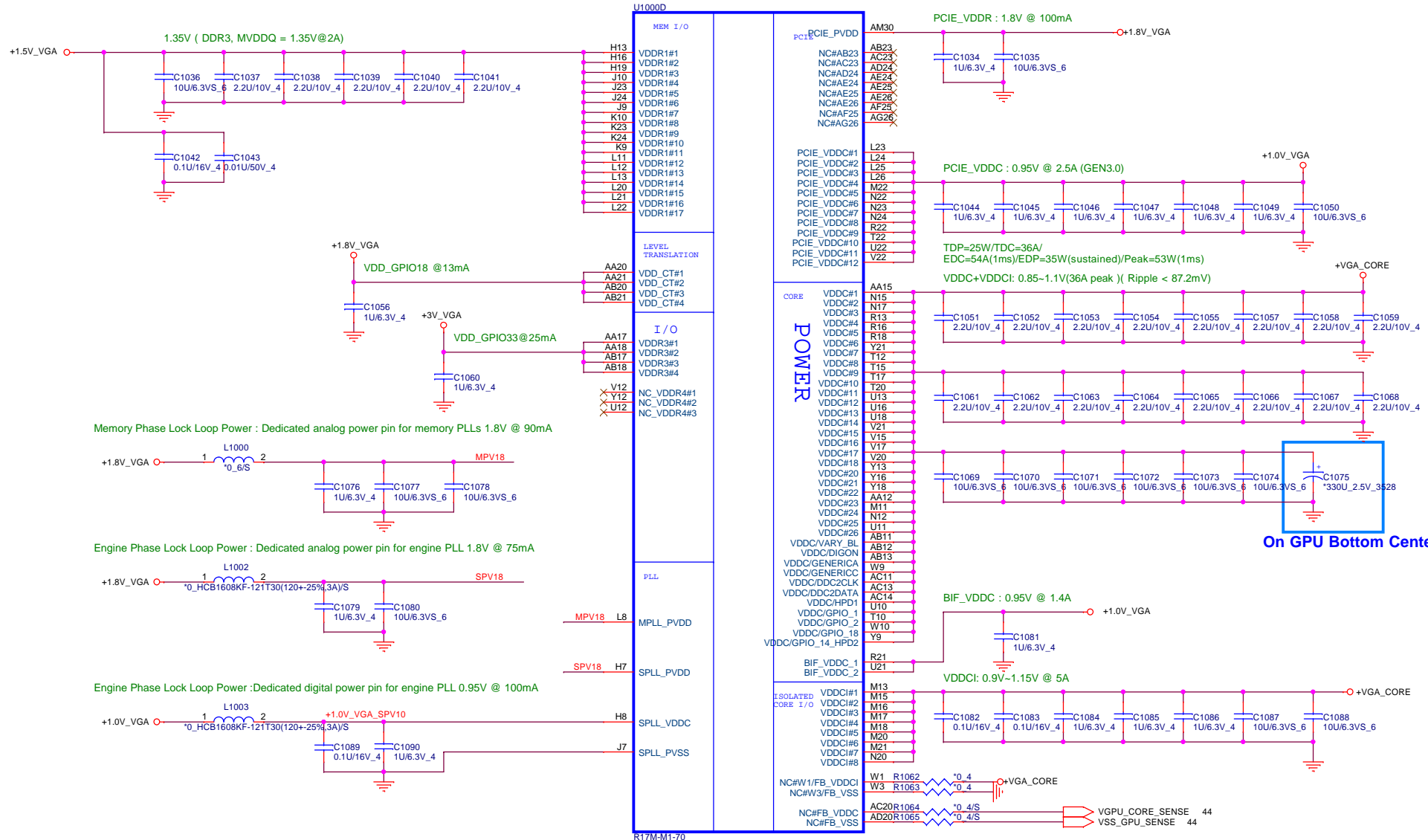
POWER DOWN



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Quanta Computer Inc.

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13,14,43,44,47 +3V_VGA
13,14,43,44,47 +1.8V_VGA
17,18,19,43,46 +1.5V_VGA
13,43,47 +1.0V_VGA
43,44,45 +VGA_CORE



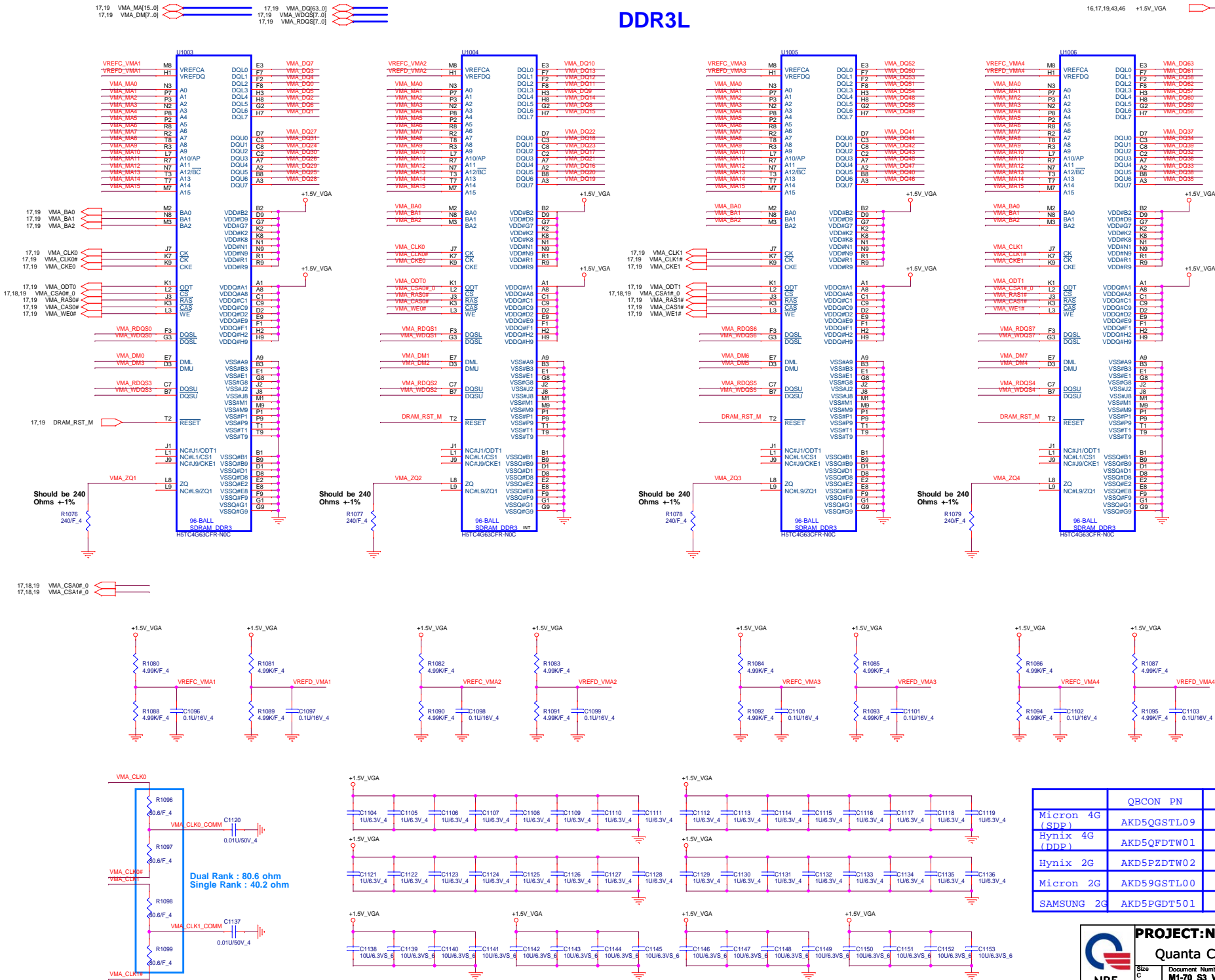
PROJECT:NFLP-G94A

Quanta Computer Inc.

Size	Document Number	Rev
	M1-70_S3_POWER	1A
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DDR3L

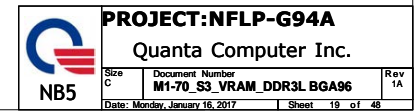


PROJECT:NFLP-G94A

Quanta Computer Inc.



Size C Document Number M1-70_S3_VRAM_DDR3L BGA96 Rev 1A
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The schematic diagram illustrates the power supply section. A +3V input is connected to a fuse F4503 (1.5A 6V POLY). The output of the fuse is connected to a network of resistors R4522 and R4523 (both 0.8S) and capacitors C4526, C4516, and C4517. The network is designed to provide a +3V_TS output and a +3V_CAM output, with decoupling capacitors C4516 (0.01uF 50V_4) and C4517 (4.7uF 6.3V_5) connected to ground.

[illegible]

TP_ID	Definition
0	14" 17"
1	15"

12/2: SI add

4	INT_EDP_TXP0	C4513	0.1u"16V 4	INT_EDP_TXP0_0
4	INT_EDP_TXN0	C4514	0.1u"16V 4	INT_EDP_TXN0_0
4	INT_EDP_TXP1	C4515	0.1u"16V 4	INT_EDP_TXP1_0
4	INT_EDP_TXN1	C4518	0.1u"16V 4	INT_EDP_TXN1_0

4 INT_eDP_AUXN C4524 0.1u/16V 4 INT_eDP_AUXN

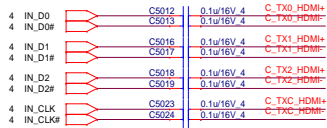
4 INT_eDP_AUXP C4525 0.1u/16V 4 INT_eDP_AUXP

4 APU_DPST_PWM R4515 10 5% 4 BRIGHT

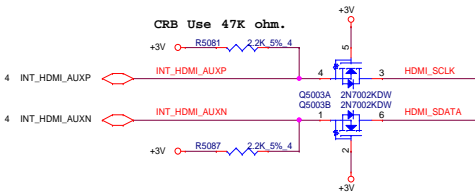
4 APU_LVDS_BLON R4516 0 4/S LVDS_BLON1

4 APU_DISP_ON R4517 0 4/S DISP_ON

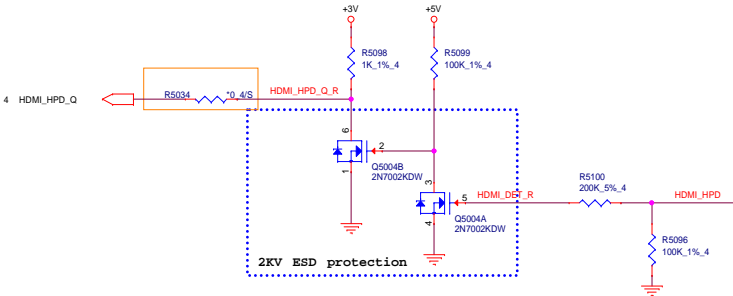
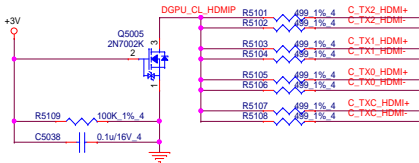
HDMI CONN



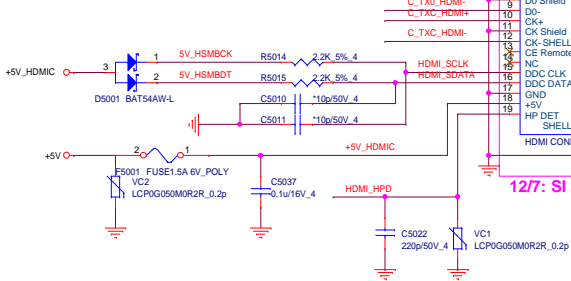
HDMI SMBus isolation



Close to HDMI connector

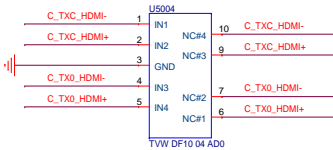
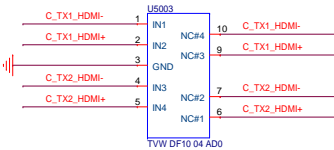


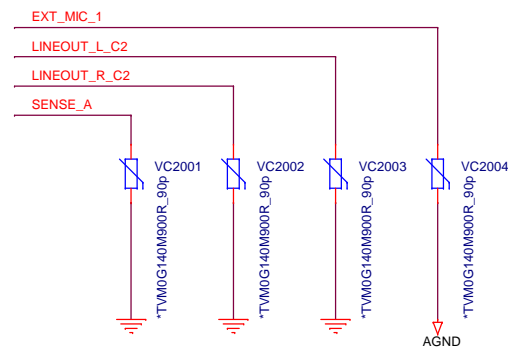
For EMI Solution



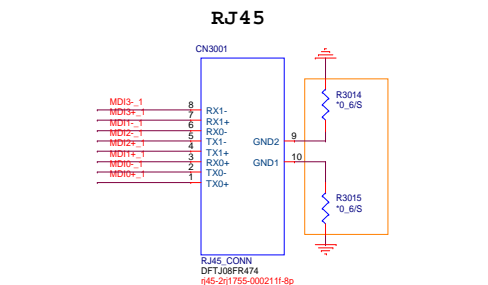
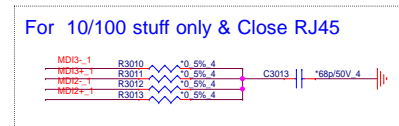
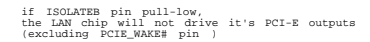
12/7: SI modify FP for SMT

For ESD Solution





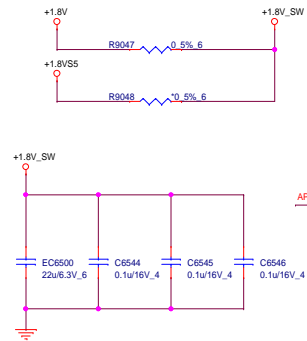
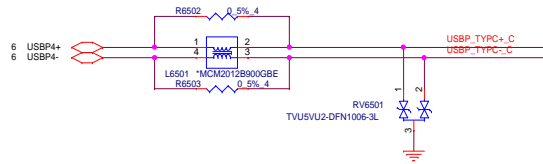
Size B	Document Number Audio Jack	Rev 1A
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12/2: SI modify For 25 pin connect GND:

USB3 SW - PI2EQX632 + USB TYPE-C - TPS25810

USB2.0



SEL = High, Channel 1 active

SEL = NC, Both Channels are Power-down

SEL = Low, Channel 2 active

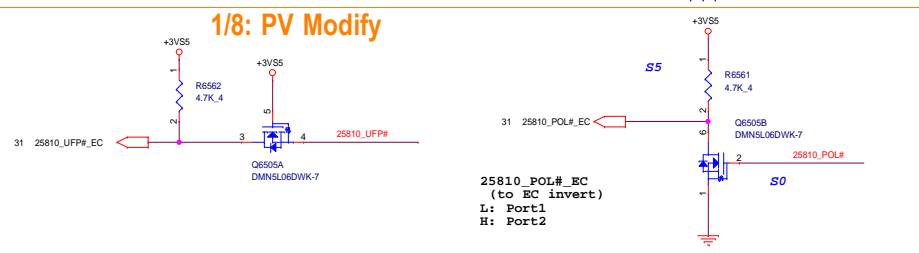
11/27: SI change Pin define & Symbol error

1/12: Add Net name

USB3.0 SW

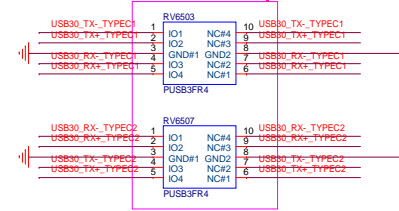
12/6: SI change U6501 FP for SMT

1/8: PV Modify

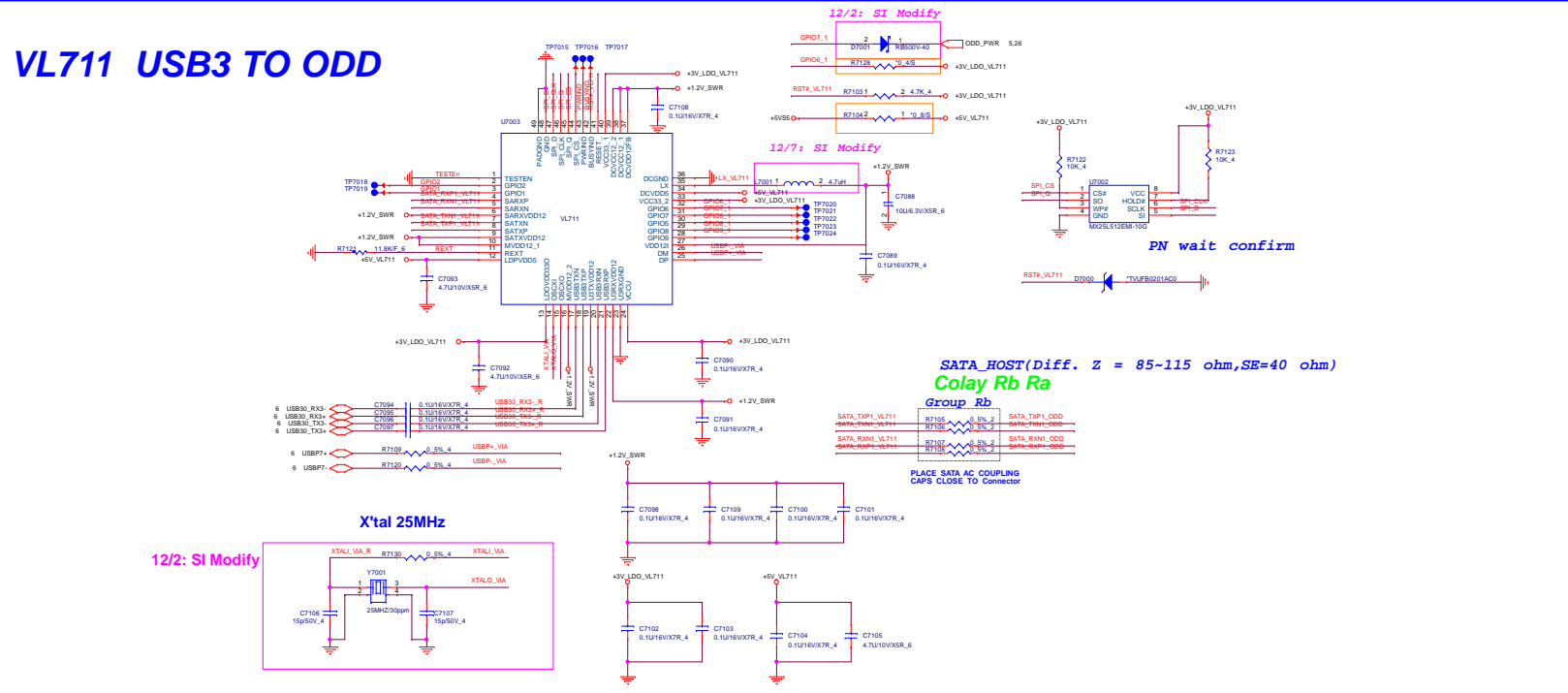


TPS25810 Port	CC1	CC2	OUT	VCONN On CC1 or CC2	POLs	UFPs	AU/DIOs	DEBUg
Nothing Attached	OPEN	OPEN	OPEN	NO	H-Z	H-Z	H-Z	H-Z
UFP Connected	Rd	OPEN	IN1	NO	H-Z	LOW	H-Z	H-Z
UFP Connected	OPEN	Rd	IN1	NO	LOW	LOW	H-Z	H-Z
Powered Cable/No UFP Connected	OPEN	Ra	OPEN	NO	H-Z	H-Z	H-Z	H-Z
Powered Cable/UFP Connected	Rd	Ra	IN1	CC2	H-Z	LOW	H-Z	H-Z
Powered Cable/UFP Connected	Ra	Rd	IN1	CC1	LOW	LOW	H-Z	H-Z
Debug Accessory Connected	Rd	Rd	OPEN	NO	H-Z	H-Z	LOW	H-Z
Audio Adapter Accessory Connected	Ra	Ra	OPEN	NO	H-Z	H-Z	LOW	H-Z

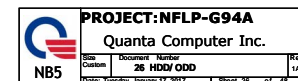
TYPE C USB3.0 ESD



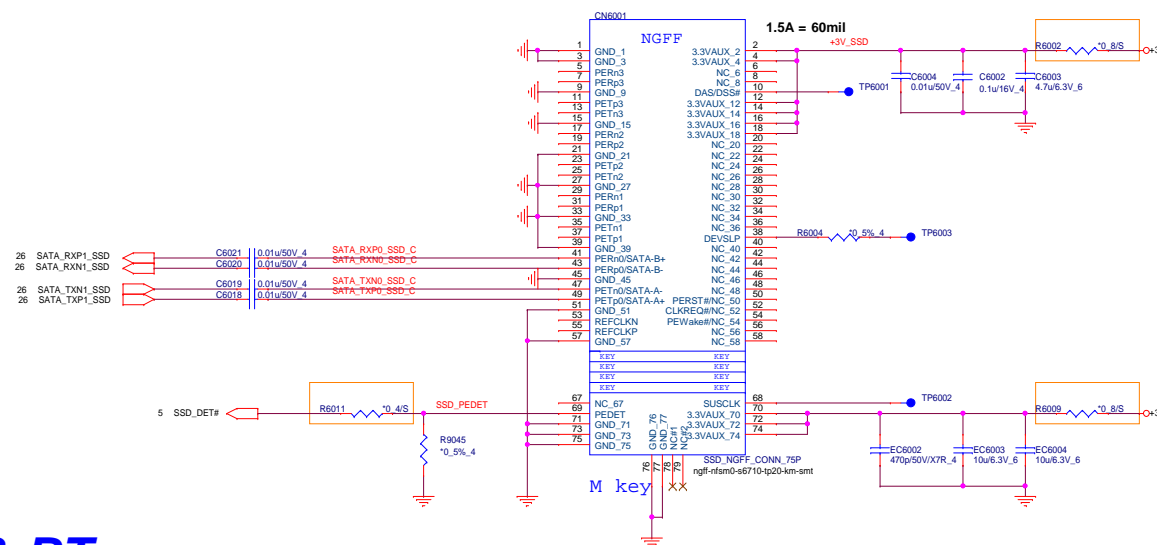
12/6: SI Modify FP/PN



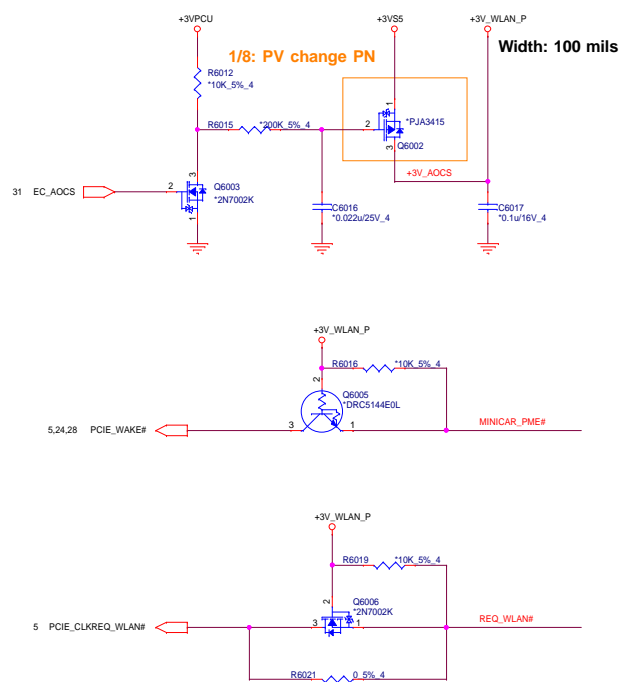
17.3" ODD PN change to DFFC18FR044,FP the same



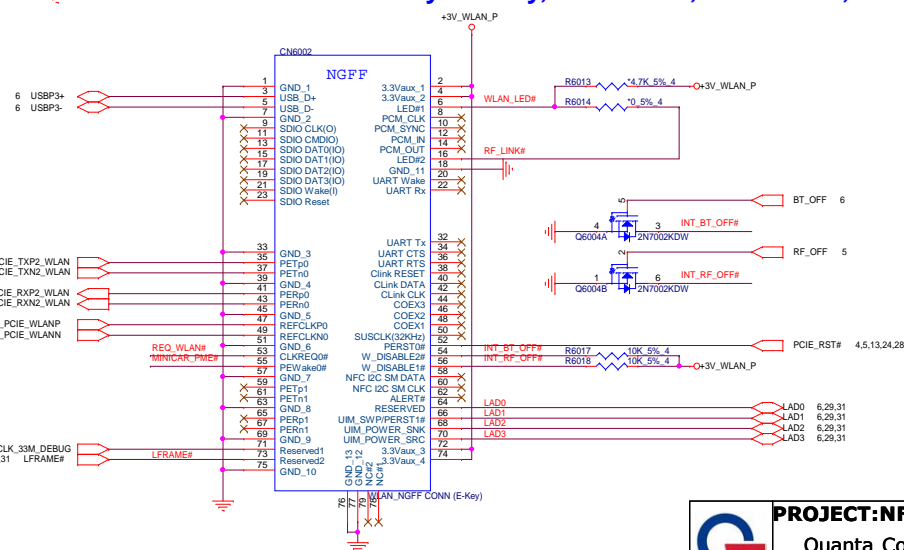
Conn PN FP OK! Libray modify, add Pin78,79



WLAN & BT

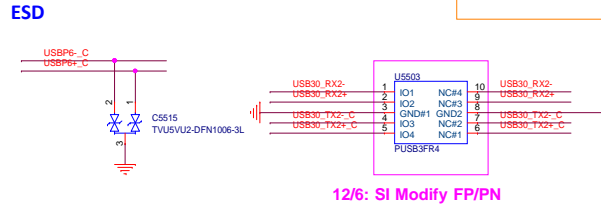
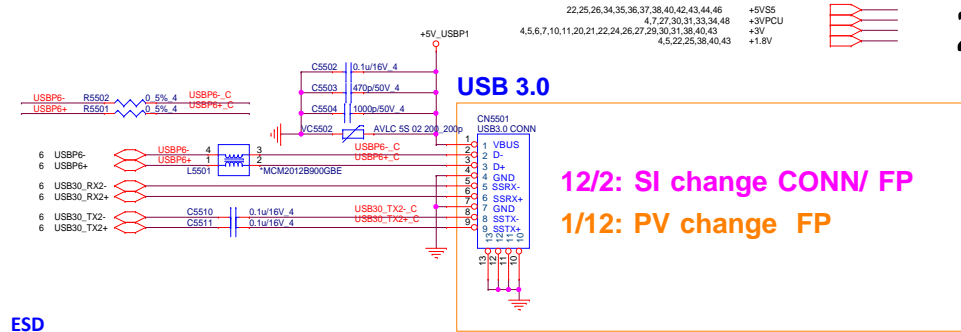
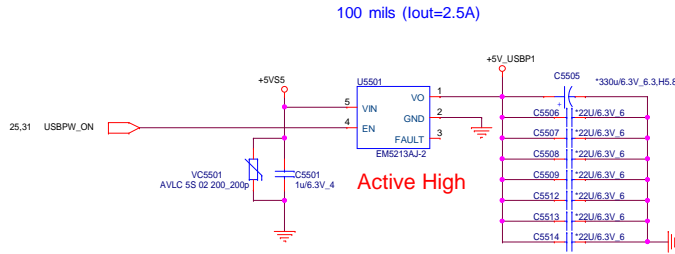


Conn PN FP OK! Library modify, Del 24~31, add Pin78,79



For 15.6" / 17.3" 2SPD

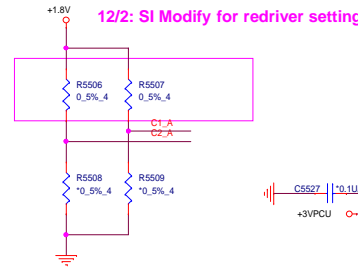
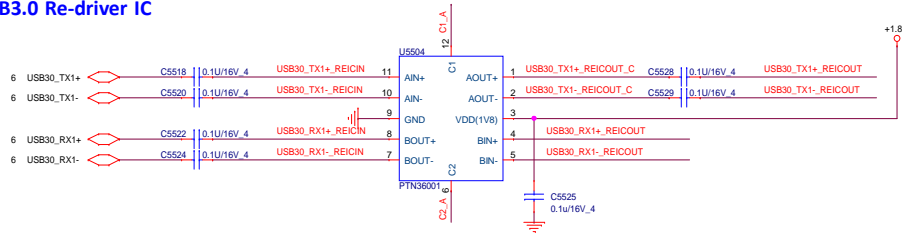
28



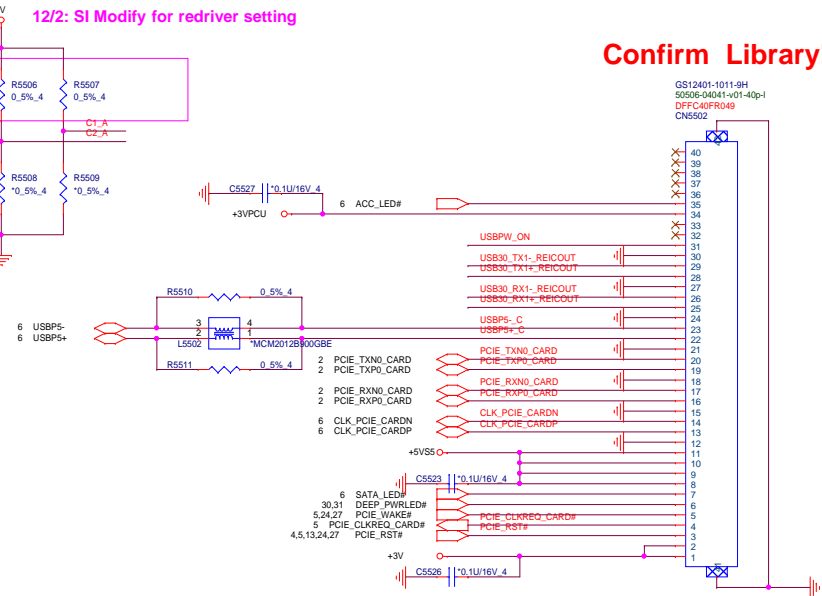
USB3.0

USB3.0 Re-driver IC

USB3.0 re-driver IC



Confirm Library!



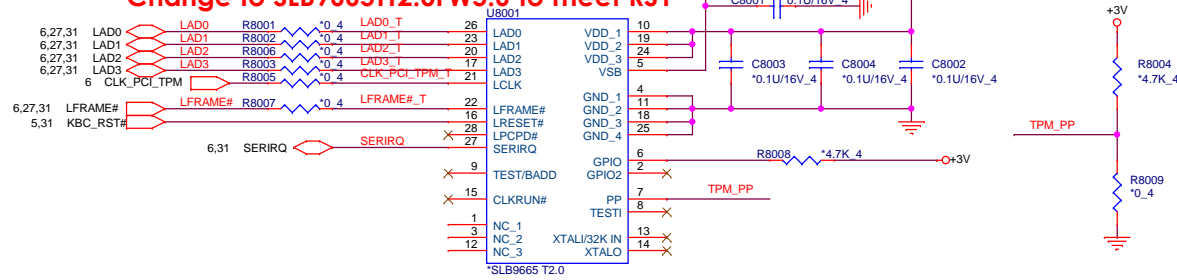
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Date: Monday, January 16, 2017	Sheet 28 of 48	

TPM (2.0)

Change to SLB9665TT2.0FW5.6 to meet RS1



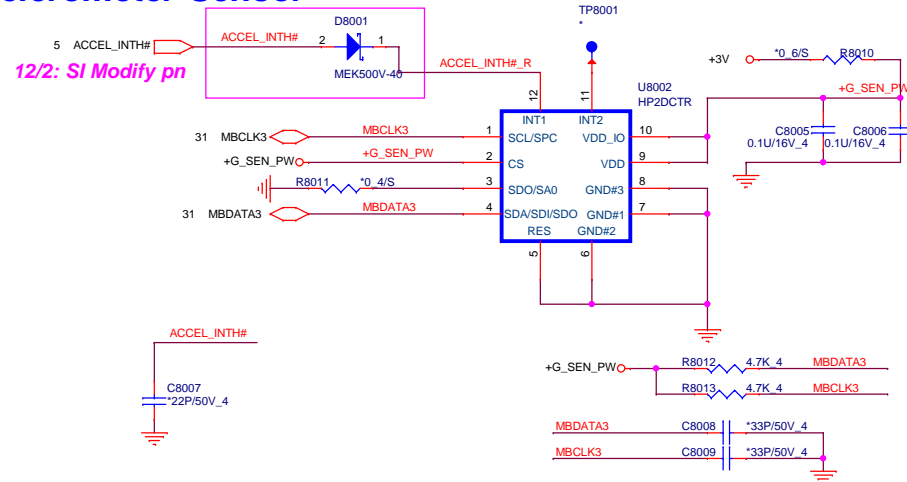
4,5,6,7,10,11,20,21,22,24,26,27,28,30,31,38,40,43

+3V_WLAN_P
+3V



29

Accelerometer Sensor

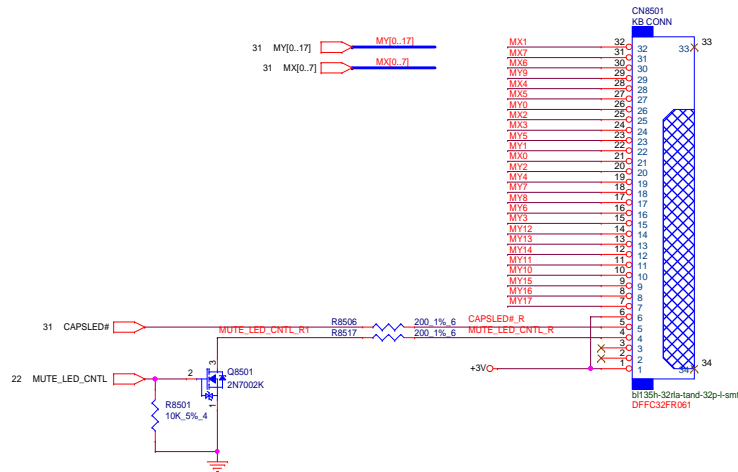


IR CAM on Page20

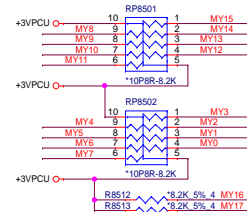
KEYBOARD CONN

Conn Wait confirm FP!!

Touch Pad CONN

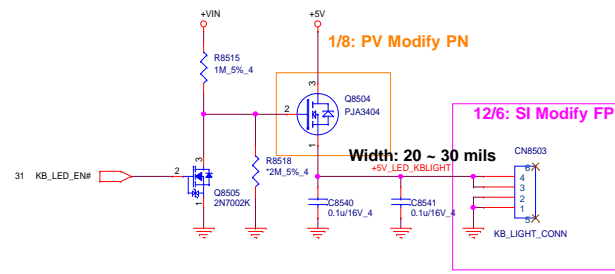


KEYBOARD PULL-UP

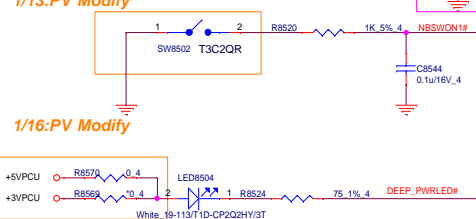


MY8	C8506	220p/50V_4
MY9	C8507	220p/50V_4
MY10	C8508	220p/50V_4
MY11	C8509	220p/50V_4
MY8	C8510	220p/50V_4
MY9	C8512	220p/50V_4
MY10	C8513	220p/50V_4
MY11	C8515	220p/50V_4
MY1	C8516	220p/50V_4
MY2	C8517	220p/50V_4
MY3	C8520	220p/50V_4
MY0	C8521	220p/50V_4
MX4	C8522	220p/50V_4
MX6	C8523	220p/50V_4
MX0	C8524	220p/50V_4
MX2	C8525	220p/50V_4
MX7	C8526	220p/50V_4
MX0	C8527	220p/50V_4
MX5	C8528	220p/50V_4
MX1	C8529	220p/50V_4
MY12	C8530	220p/50V_4
MY13	C8531	220p/50V_4
MY14	C8533	220p/50V_4
MY15	C8534	220p/50V_4
MY16	C8536	220p/50V_4
MY17	C8537	220p/50V_4

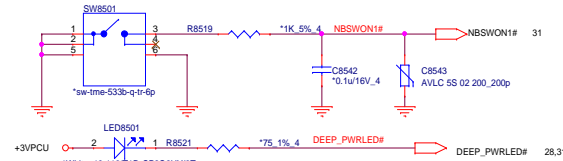
KB LIGHT CONN



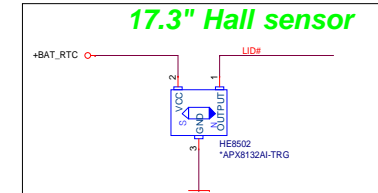
15.6" SW & LED



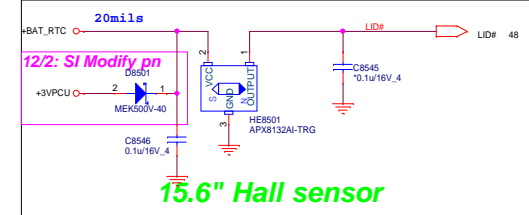
17.3" SW & LED



17.3" Hall sensor

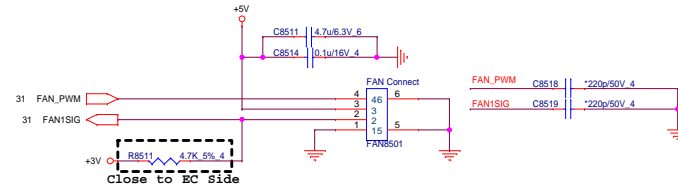


15.6" Hall sensor



FAN CONN

confirm Library



PWR Button & LED & HALL IC



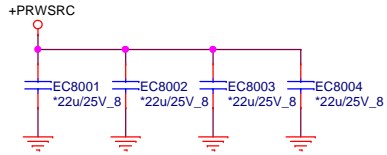
PROJECT: NFLP-G94A

Quanta Computer Inc.

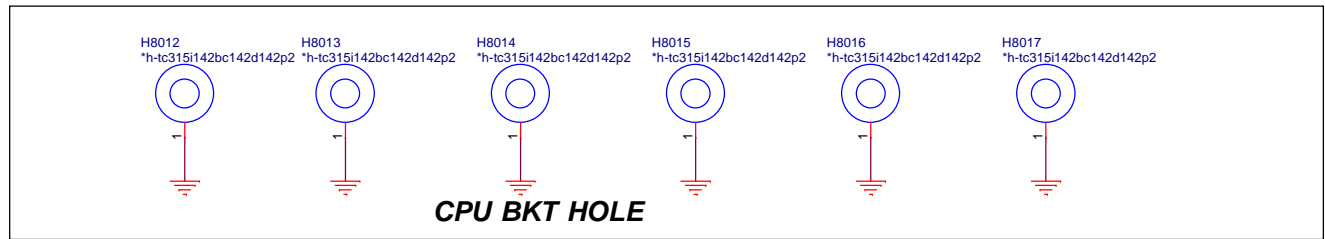
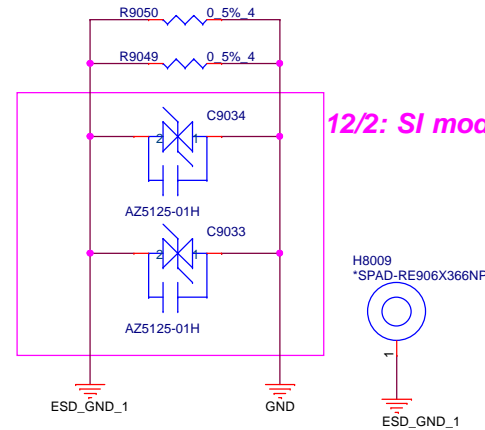
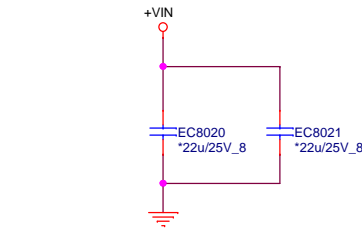
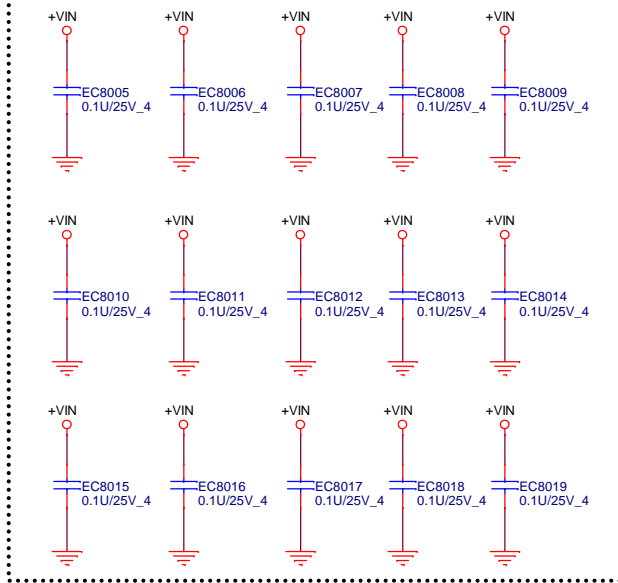
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EMI CAPs

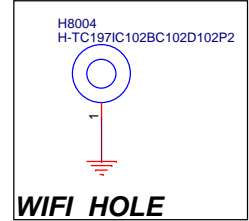
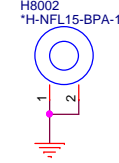
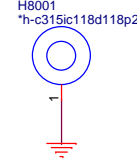
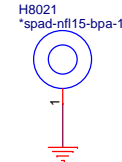
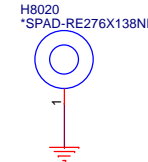
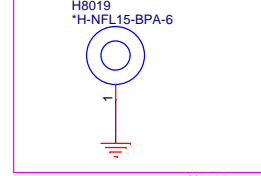
For ISN



Place on +VIN Path

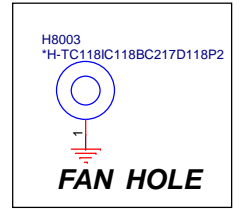
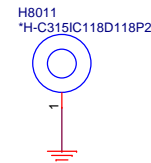
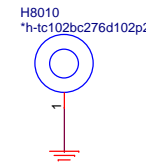
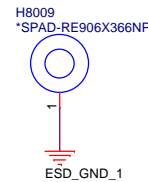
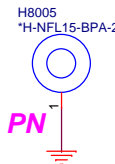
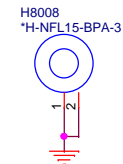
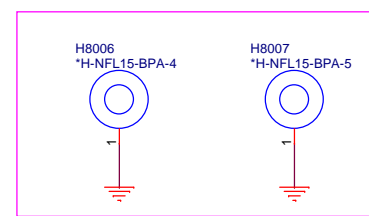


12/6: SI modify PN



WIFI HOLE

12/6: SI modify PN



FAN HOLE



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Quanta Computer Inc.

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B	EMI CAP/HOLES	1A
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NFLP-15.6"

DC JACK
45W-90W

CN1
51483-00801-V01_Header

Place this ZVS close to
Diode away +VIN

Do Not add test pad on BATDIS_G signal

$I_{dss} < 5\mu A$

Do Not add test pad on
BQBATDRV/BATDIS_ID_DOD signal

Place this ZVS close to
Far-Far away +VIN


33

ZVS close to DC jack

3S1P 41Whr

Place this cap
close to EC

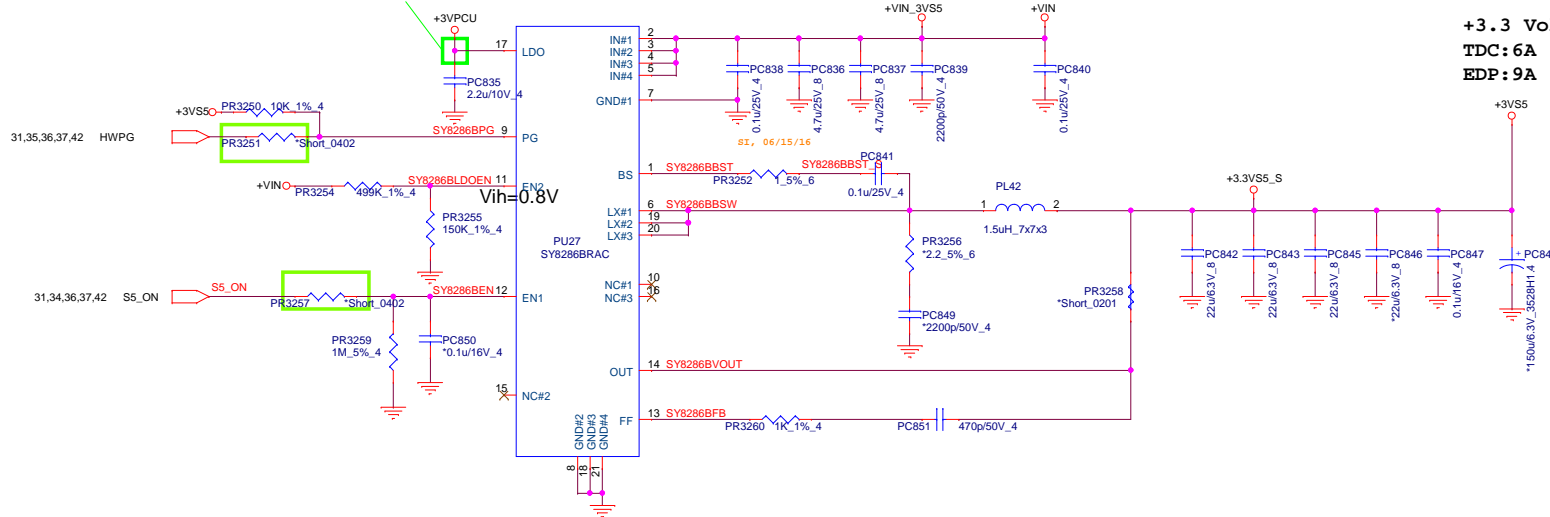
Set MAX charge I to 5A

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4,7,27,28,30,31,33,48 +3VPCU
22,30,31,33,43,47 +5VPCU

20,30,32,33,35,37,38,39,40,41,44,45,46 +VIN
5,6,7,25,27,30,31,35,37,42,43,44,47 +3VS5
22,25,26,28,35,36,37,38,40,42,43,44,46 +5VS5

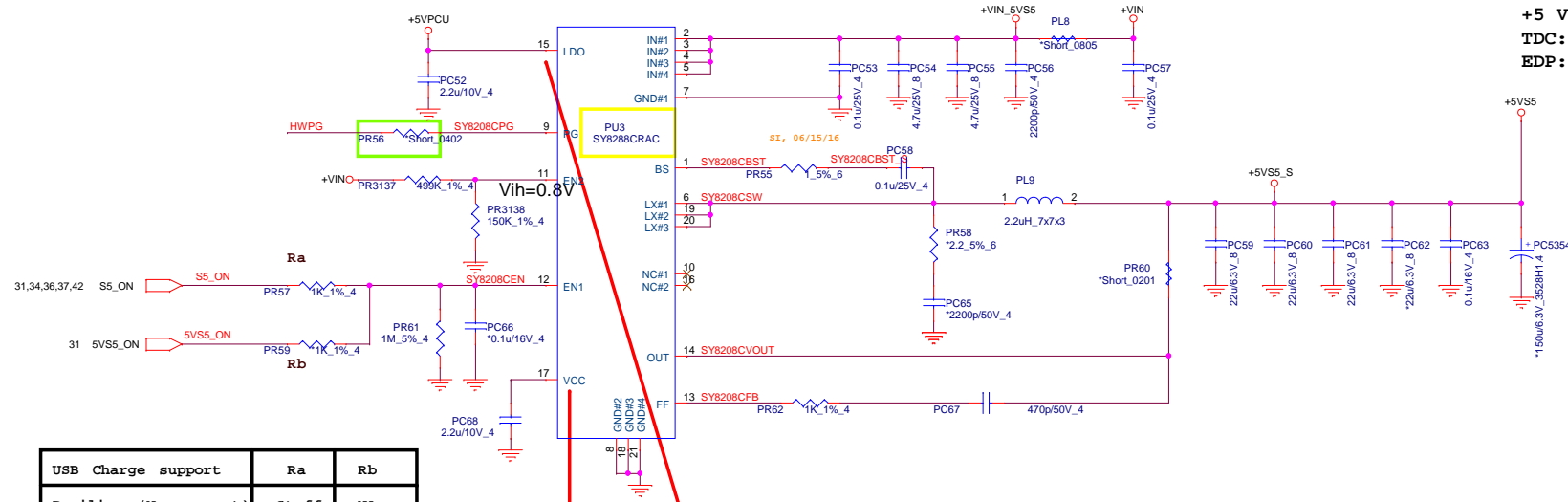
Do Not add test pad on LDO pin



+3.3 Volt +/- 5%
TDC: 6A
EDP: 9A

Vih=0.8V

Do Not add test pad on VCC & LDO pin



+5 Volt +/- 5%
TDC: 7A
EDP: 9A

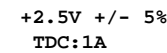
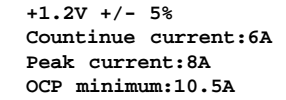
Vih=0.8V

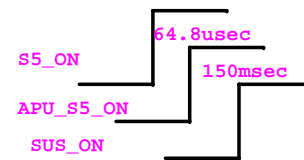
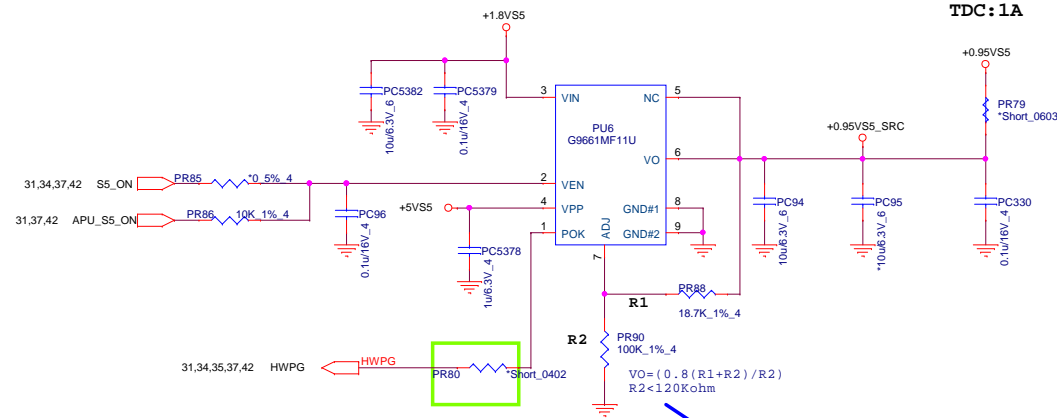
USB Charge support	Ra	Rb
Pavilion (No support)	Stuff	NA
Envy (Support)	NA	Stuff

Do Not add test pad on VCC & LDO pin

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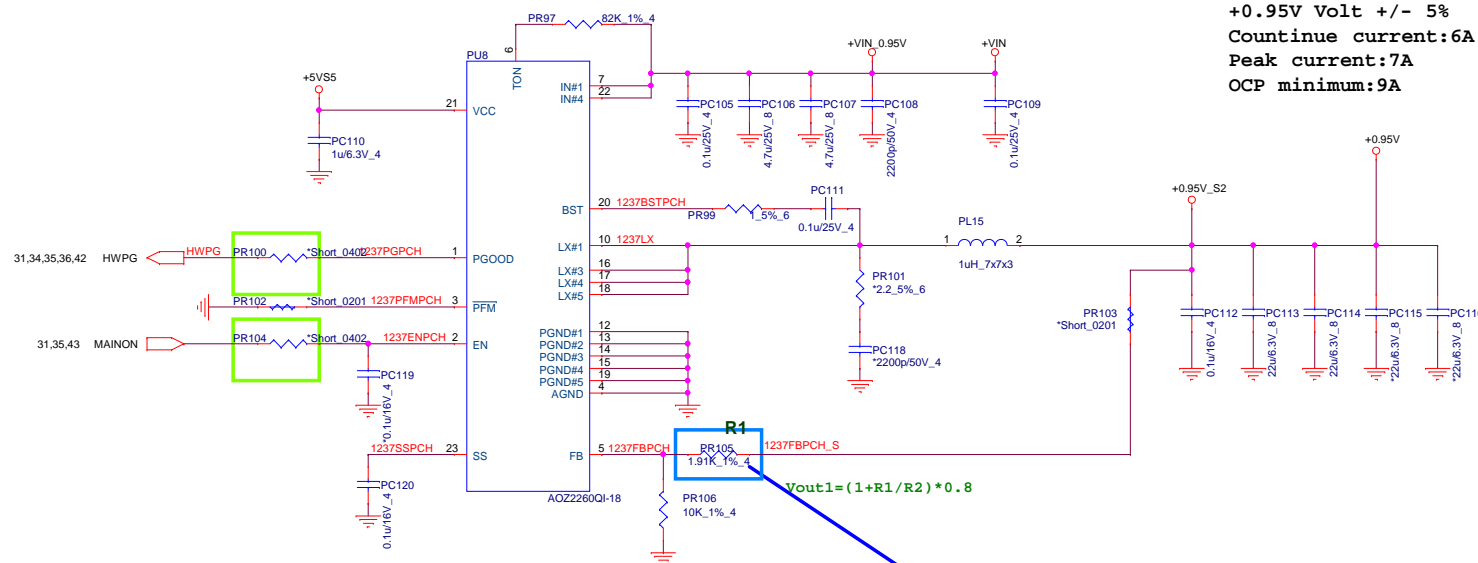




	R1		
Stoney/Bristol	18.7K	CS31872FB19	0.95V
	31.6K	CS33162FB14	1.05V

Bristol VDDP=1.05V
Stoney VDDP=0.95V

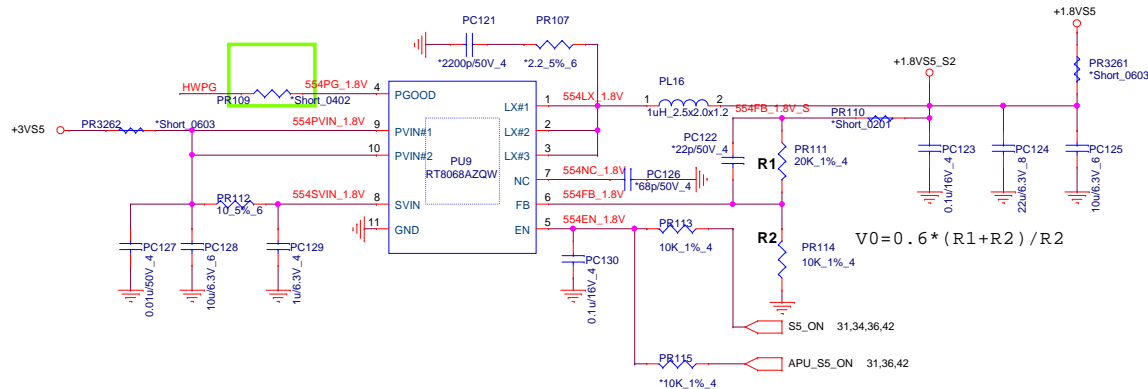
20,30,32,33,34,35,38,39,40,41,44,45,46 +VIN
2,6,7 +0.95V
5,7,25,36,43,47 +1.8VS5

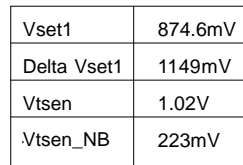


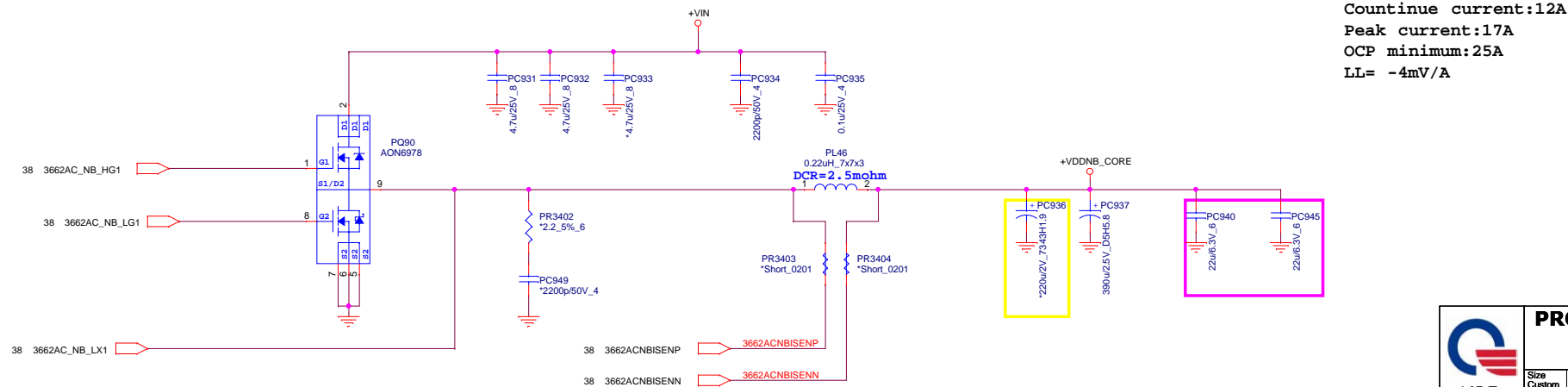
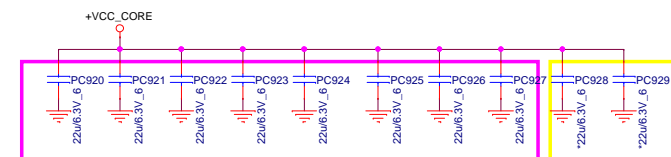
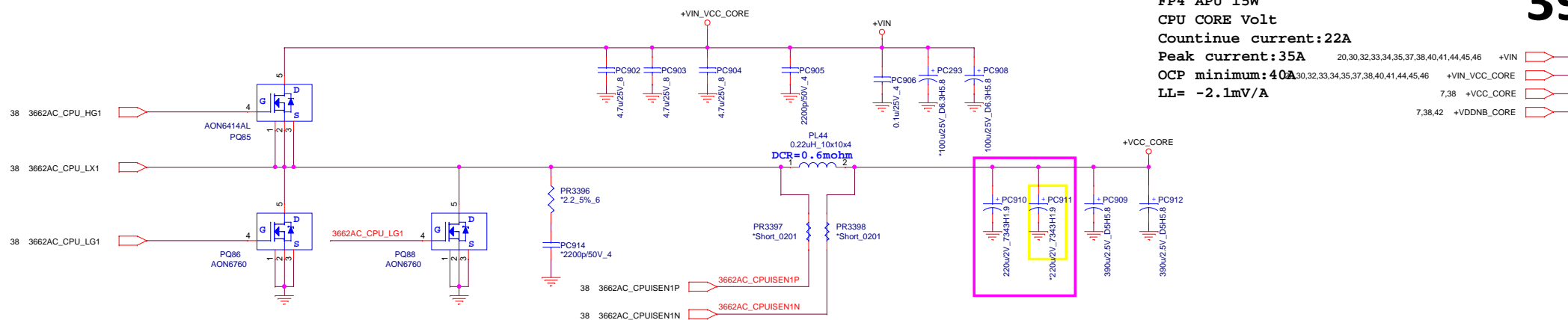
Vo	Rton
0.95V	82k
1V	84.5k
1.05V	95.3k
1.35V	113k
1.5V	127k

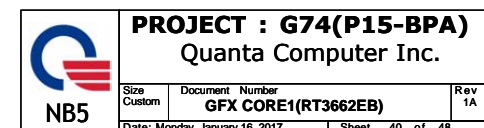
	R1		
Stoney / Bristol	1.91K	CS21912FB13	0.95V
	3.16K	CS23162FB04	1.05V

1.8VS5 +/- 3%
TDC: 3A
EDP: 4A



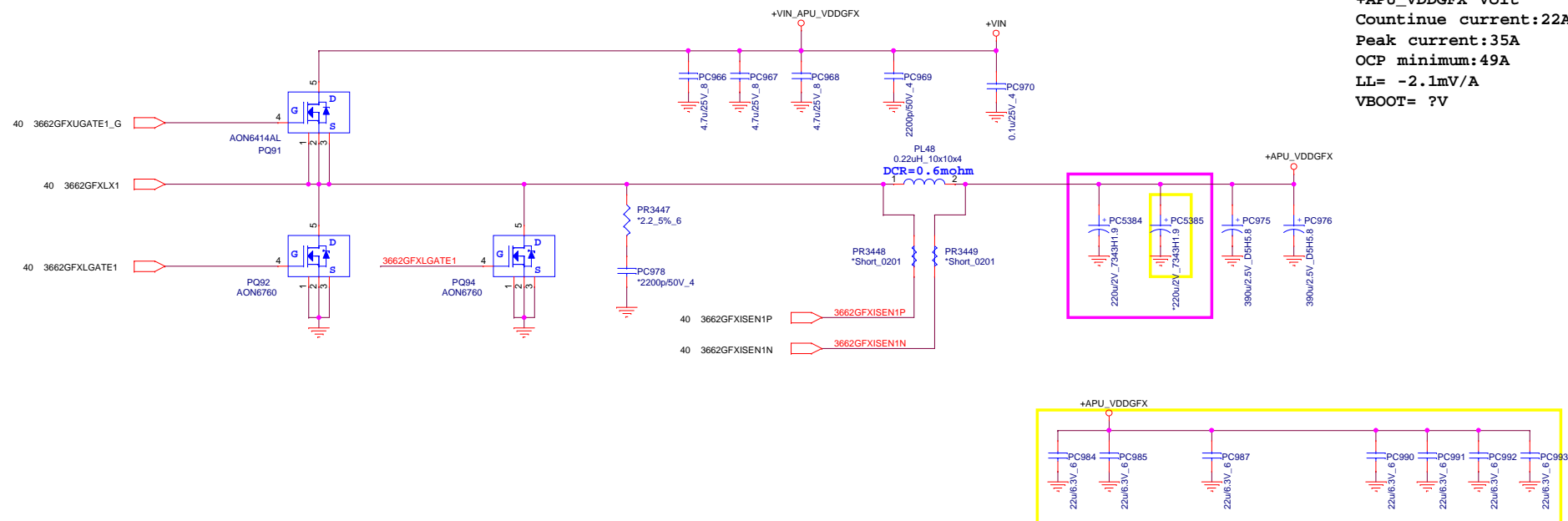


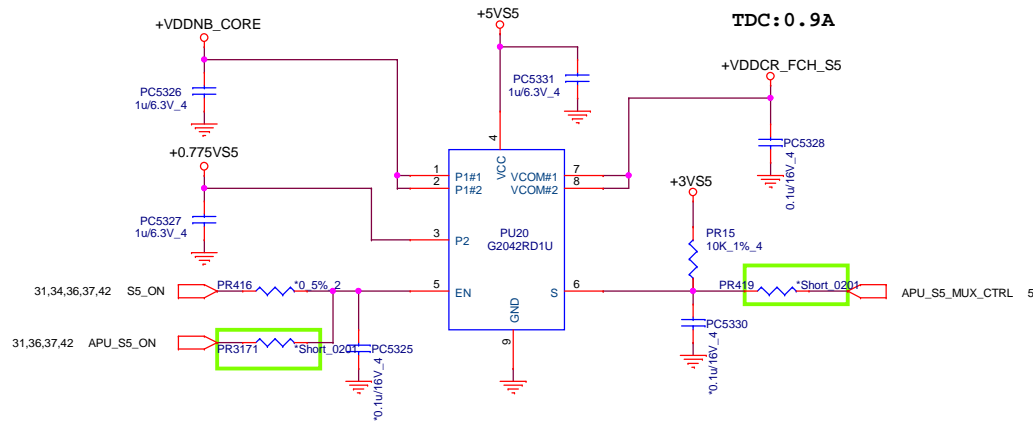




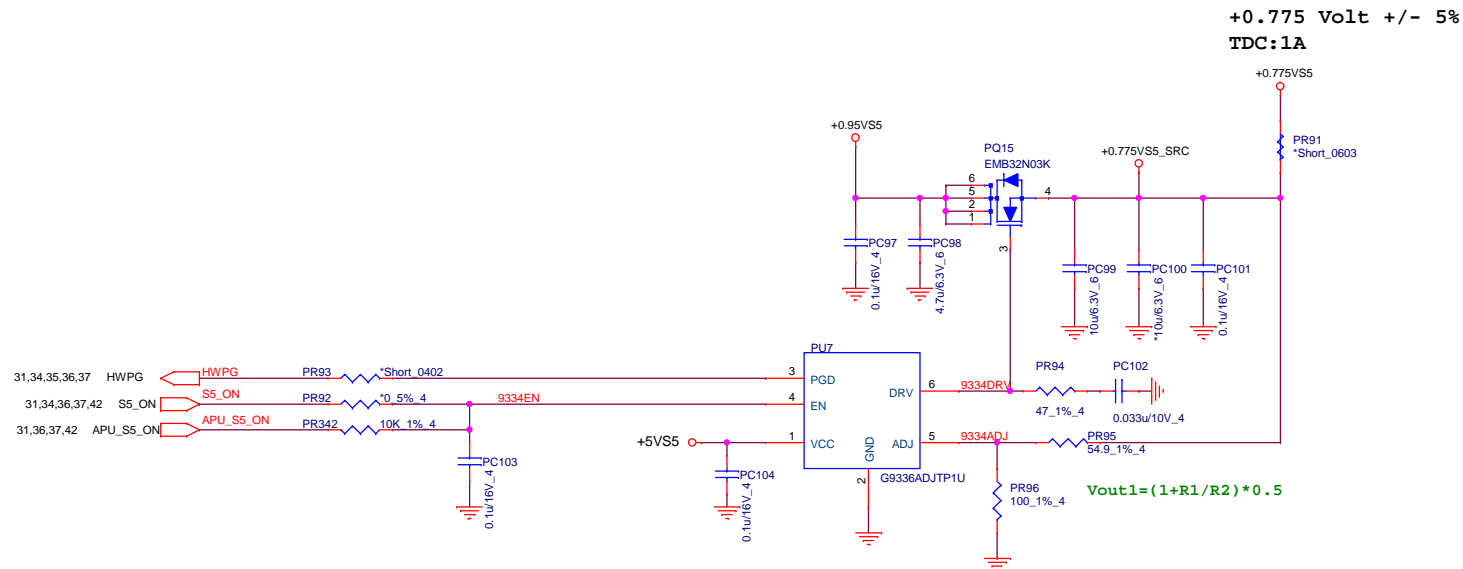
CPU	Page 40 & Page 41
Bristol	Stuff
Stonley FP4,FT4	Unstuff

20,30,32,33,34,35,37,38,39,40,44,45,46 +VIN
 20,30,32,33,34,35,37,38,39,40,44,45,46 +VIN_APU_VDDGFX
 7,40 +APU_VDDGFX



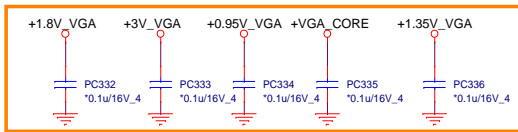


EN	SEL	VIN1	Vo
0	X	0.775V~1.2V	0V
1	0	<0.775V	0.775V
1	0	>0.775V	VDDNB
1	1	0.775V~1.2V	VDDNB

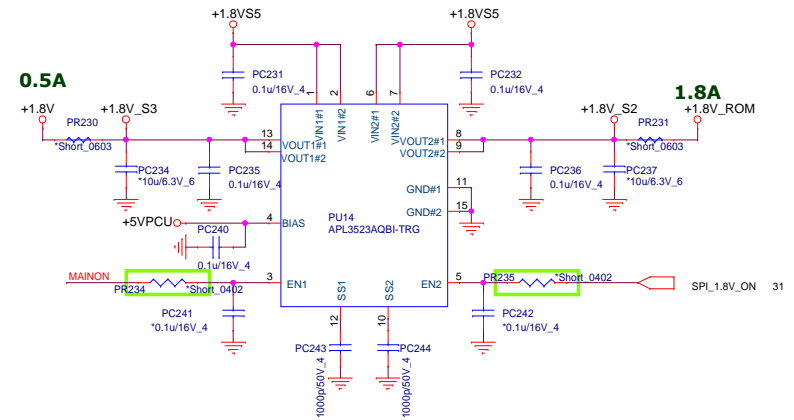
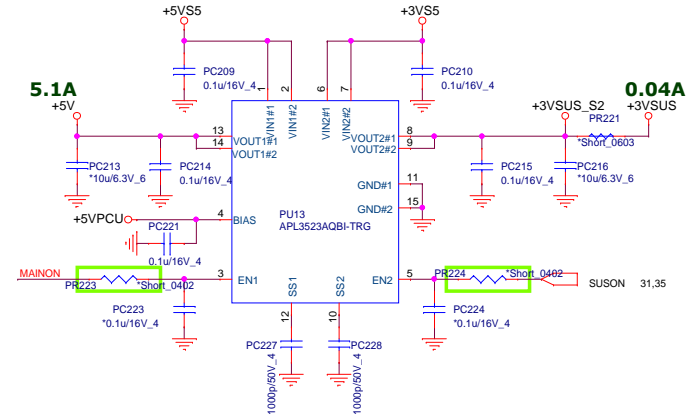
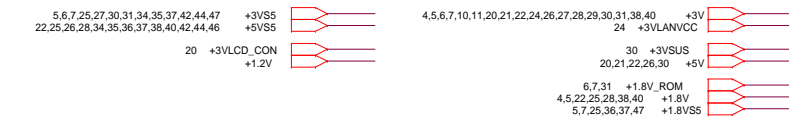
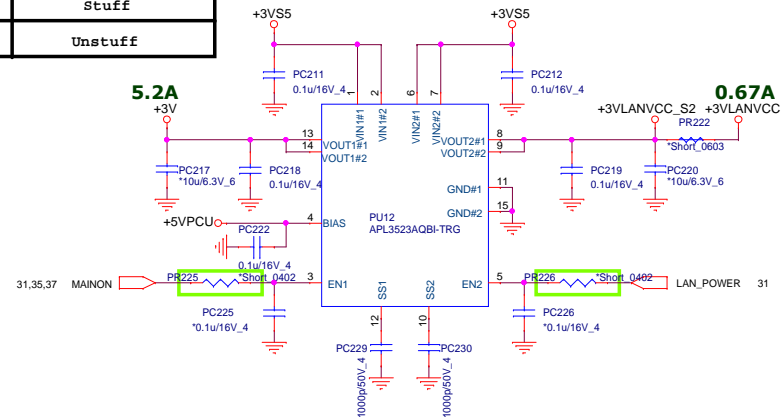


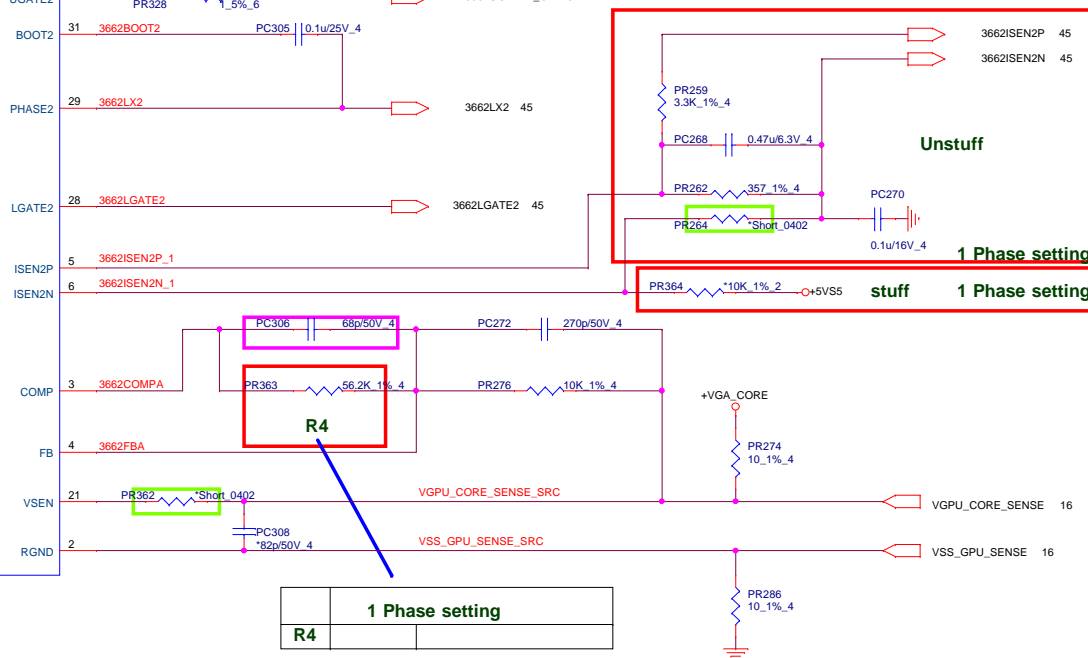
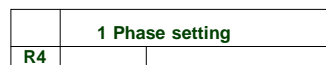
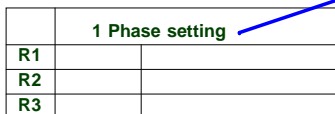
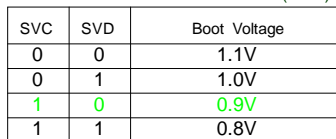
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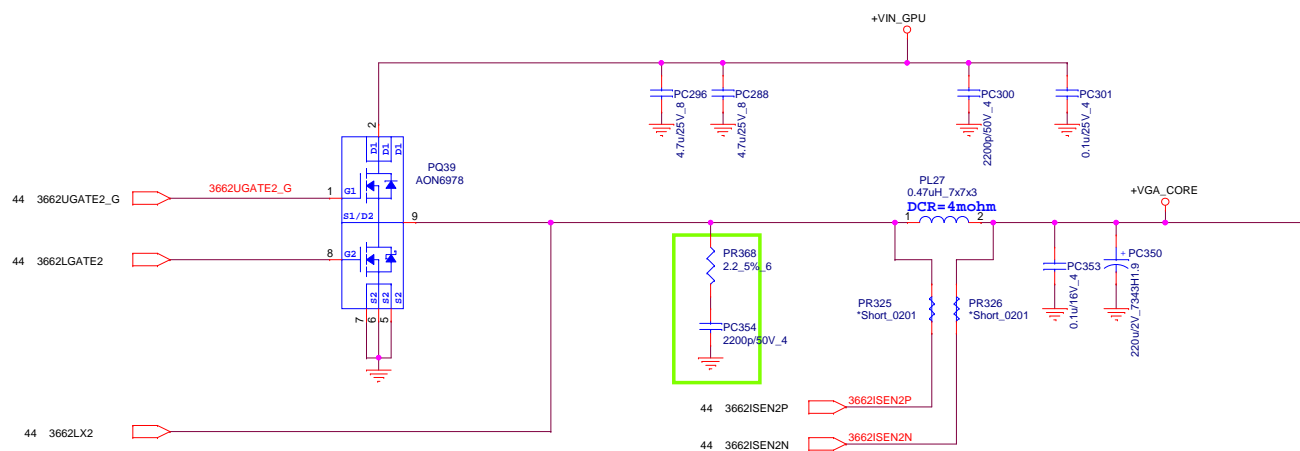
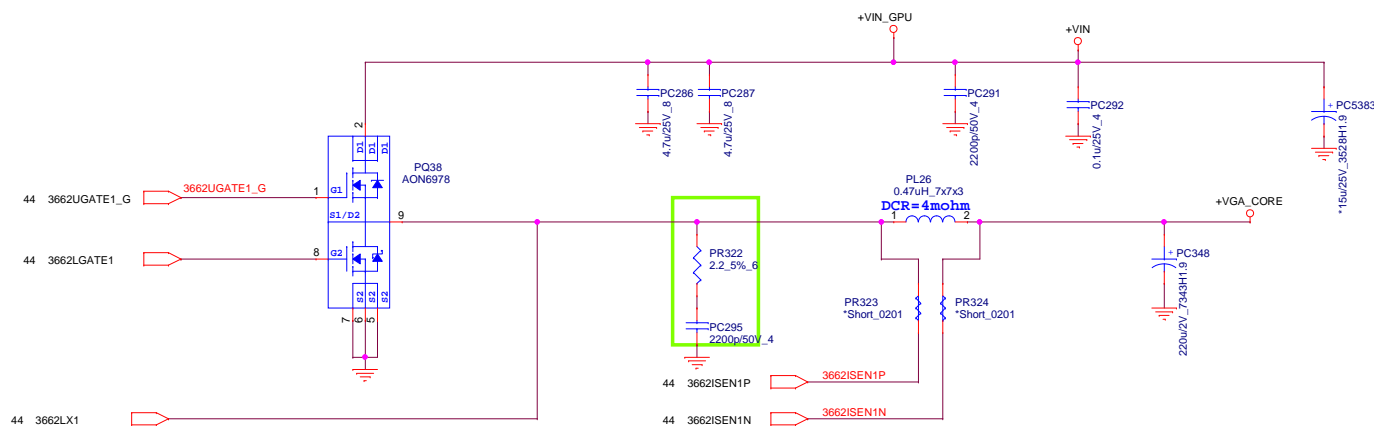
UMA only	Stuff
discrete	Unstuff

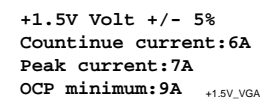




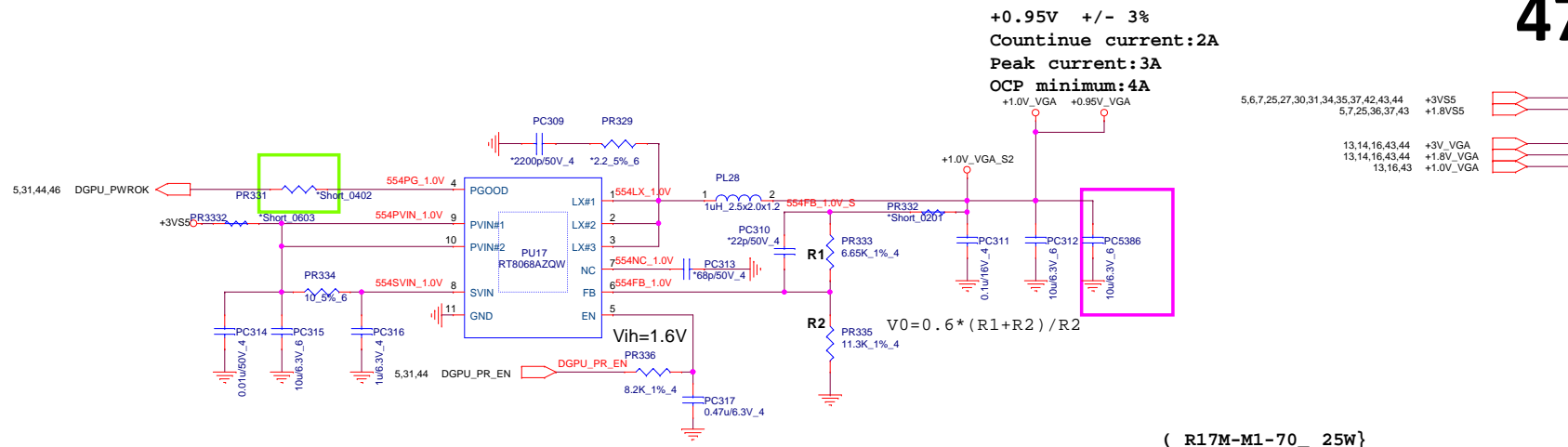
20,30,32,33,34,35,37,38,39,40,41,44,46 +VIN
 20,30,32,33,34,35,37,38,39,40,41,44,46 +VIN_GPU
 16,43,44 +VGA_CORE

VGACORE (R17M-M1-70_ 25W/38W(1ms))
Countinue current:28A
 Peak current=38A (1ms)
 PHOCP_TDC=40A (soft-start only)
 OCP_SPIKE=55A(1ms)
 Boot VID=0.9V
 LL=1m V/A

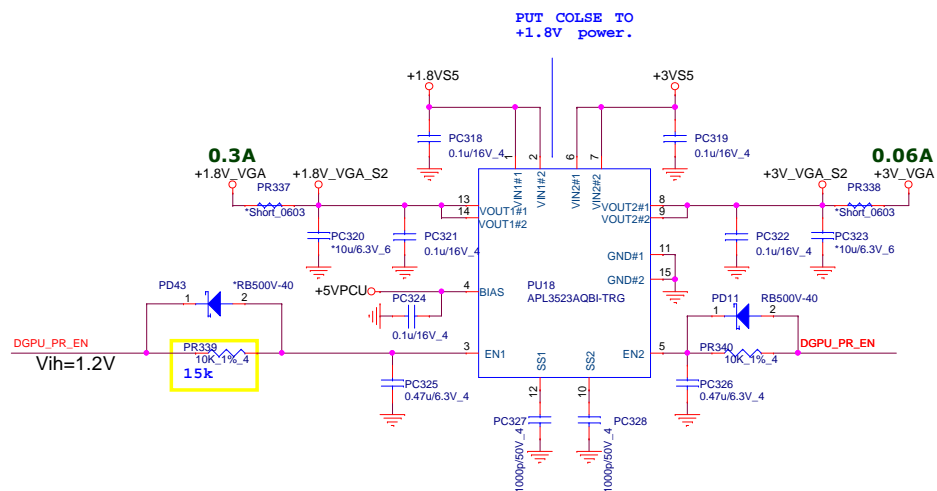




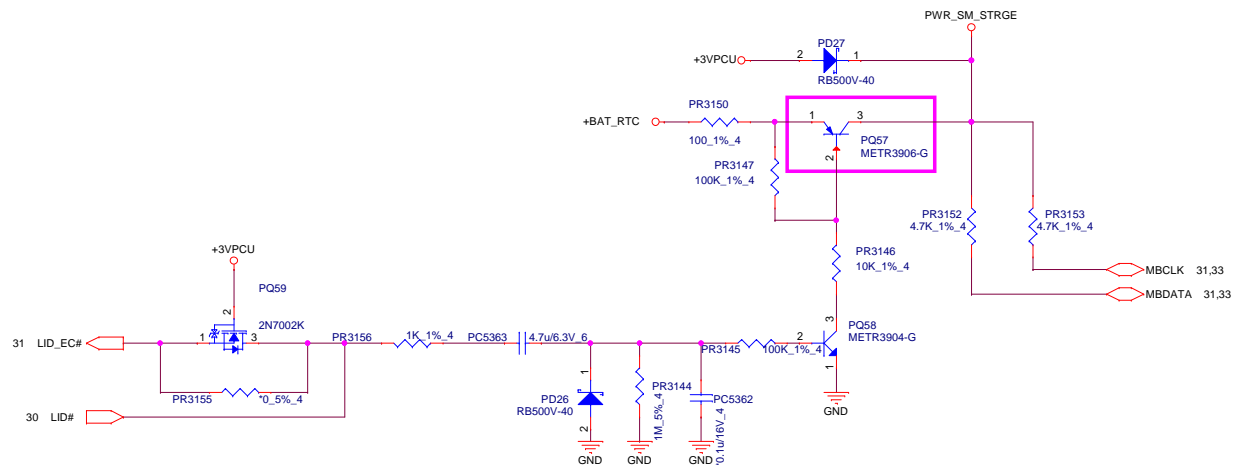
Vo	Rton
0.95V	82k
1V	84.5k
1.05V	95.3k
1.35V	113k
1.5V	127k



+3V_VGA
 +1.8V_VGA & +0.95V_VGA
 +VGA_CORE & +1.35_VGA



+3V_VGA
 +0.95V_VGA
 +VGA_CORE & +1.35_VGA
 +1.8V_VGA



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